Fabrication and Characterization of Diamond Field-Effect Transistors

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Abstract:

The next generation of communication technology requires materials that can handle higher frequency and higher power. Diamond's excellent physical properties, such as high band-gap, high breakdown field, and the highest thermal conductivity of all materials, make it ideal for communication applications. Improving diamond field-effect transistor (FET) performance will make diamond viable for such applications. We fabricated and characterized hydrogen-terminated diamond (H-diamond) FETs with an Al_2O_3 gate insulator using laser lithography, e-beam lithography, ozonolysis, e-gun sputtering, atomic layer deposition, microscopy, annealing, and FET device analysis. Challenges of this process included improving the process yield and the drain current. We found that the high stability of the H-diamond surface causing the metal electrodes to easily peel off the surface, causing a low process yield. Optimization of the fabrication process and annealing improved the process yield and the drain current, respectively.

Introduction:

As communication devices advance, they require materials that operate at higher frequency and higher power, and diamond's physical properties make it an ideal material for high frequency power applications. These properties include the highest breakdown field (10 MV cm^{-1}), a wide band-gap energy (5.47 eV), the highest thermal conductivity (22 W cm^{-1} K^{-1}), and the highest carrier mobility (2200 and 1800 cm_2 V^{-1} s^{-1} for electrons and holes, respectively) [1, 2]. Improving the performance of diamond FETs would allow the next generation of communication devices to use these properties.

Diamond FETs consist of a gate, source, drain, gate insulator, and hydrogen-terminated diamond (H-diamond) surface [3], as shown in Figure 1a. This H-terminated surface provides hole carriers, and these holes allow current to flow from the drain to the source. Varying the gate voltage and the drain voltage to measure the induced drain current results in an I_d-V_d graph, as depicted in Figure 1b, and these graphs are used to characterize FET performance. FET performance is considered superior when the maximum drain current is higher. In this work, we seek to improve existing fabrication procedures to increase the maximum drain currents.

Fabrication Procedures:

Figure 2 depicts the fabrication procedures performed on H-diamond samples. We first patterned the surface to define FET areas using laser lithography. Defining FET areas involved exposing the sample to ozone in UV light. Oxygen passivated the exposed H-terminated surface, and liftoff left a surface patterned with H-terminated FET areas (Figure 2a). Next, we used e-beam lithography to obtain high resolution patterns for the source-drain electrodes. We deposited palladium (Pd), titanium (Ti), and gold (Au) by e-gun deposition (Pd and Ti acted as adhesion layers), before performing liftoff (Figure 2b). The third step consisted of depositing the gate insulator aluminum oxide (Al_2O_3) by atomic layer deposition (ALD) and defining the gate electrodes. We used laser lithography to pattern the surface, and we evaporated onto the surface Ti (as an adhesion layer) and Au (Figure 2c). Liftoff revealed fully fabricated diamond FETs (Figure 2d).

The previous and improved procedures were alike, except for the third and fourth steps. In the previous procedure, we deposited the photoresist before the Al_2O_3 and gate metal, and liftoff. However, many of the source-drain electrodes peeled off the surface, as shown in Figure 3a, nullifying 10/36 FETs.

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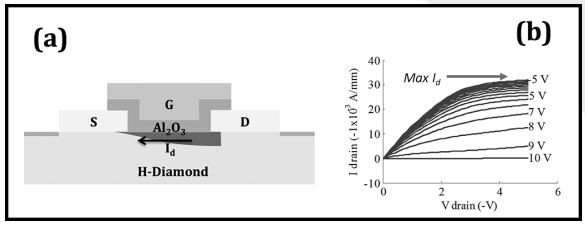

Figure 1: (a) Diamond FET. (b) I_dV_d characteristic of FETs.

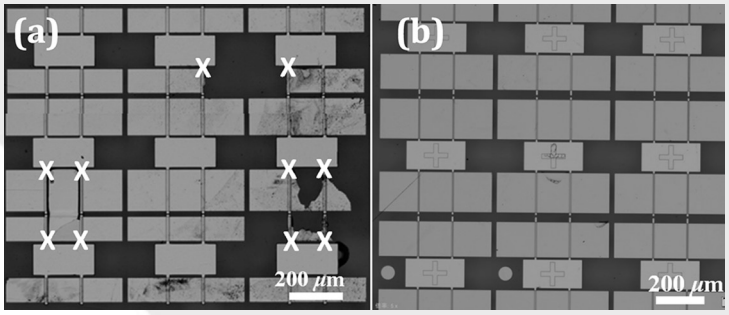

Figure 3: Sample following lift-off in (a) the previous, and (b) the improved processes.

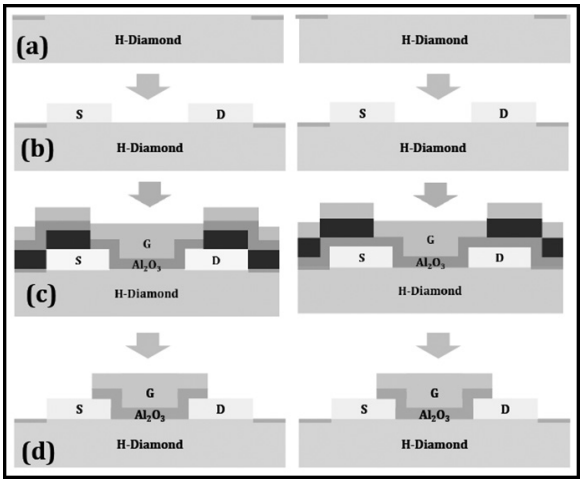

Figure 2: Previous (on left) and improved (on right) procedures for diamond FETs. (a) Defining FET areas.
(b) Defining the source-drain electrodes. (c) Depositing gate insulator and defining the gate electrodes. (d) Lift-off to form diamond FET.

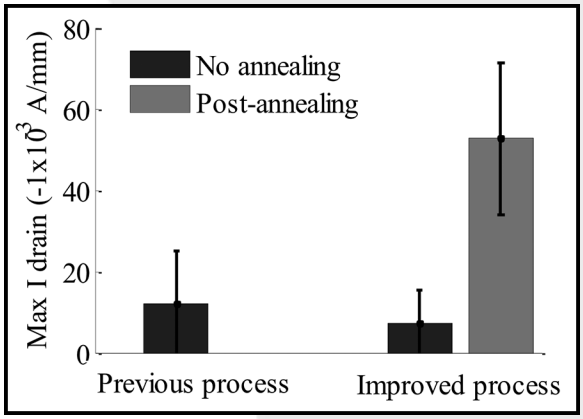

Figure 4: Maximum drain currents for the previous (n = 7) and improved (n = 8) fabrication processes.

In the improved procedure, we deposited the Al_2O_3 before the photoresist and gate metal, and liftoff. This eliminated the peel-off behavior, as shown in Figure 3b. We then annealed the improved sample at 200°C for one hour in vacuum to improve device performance.

Characterization and Results:

Varying the last steps of the procedure eliminated the peel-off behavior due to the stability of H-diamond. The source-drain electrodes were weakly attached to the H-terminated surface. The photoresist to source-drain attachment may be stronger than the source-drain to H-diamond attachment. Thus, lifting off the photoresist may also peel off source-drain electrodes. Passivating the surface with Al_2O_3 removed this effect due to the unique properties of ALD Al_2O_3. ALD Al_2O_3 is commonly used as a diamond gate insulator, because it both protects and strongly adheres to the H-terminated surface. Thus, passivating the entire surface with Al_2O_3 after defining the source-drain electrodes ensured the source-drain electrodes would not easily peel off.

Figure 4 shows the maximum drain current of the previous and improved process, and it shows the maximum drain current of the improved process post-annealing. Post-annealing significantly increased the average maximum drain currents of the procedures from 7.22 mA/mm to 52.6 mA/mm, and following annealing, one sample obtained a maximum drain current of 88.5 mA/mm. Annealing likely reduced the hole trap density in the Al_2O_3 and the interface between the Al_2O_3 and the H-diamond, although further work is needed to verify this hypothesis.

Conclusions and Future Work:

Improvements to the fabrication procedure of diamond FETs eliminated peel-off behavior, and post-annealing significantly increased the drain current of the FETs. Future research involves further investigation of the post-annealing phenomenon.

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