Investigation of TiO_2 Films Deposited by Low-Temperature ALD Process for Future CMOS

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Abstract:

Anatase-type titanium dioxide (TiO_2) thin films were investigated for their application in three dimensional (3D) integrated circuit (IC) designs. The TiO_2 films were deposited using atomic layer deposition (ALD) over other types of deposition because it offers both angstrom-order thickness resolution and the unique conformal deposition required for 3D fabrication. TiO_2 was deposited with four differing cycles resulting in four different thicknesses ranging from 3-7 nm. These samples were separately annealed at 300, 400, and 500°C. Electrical characterization revealed that only the 500°C fabrication process produced TiO_2 usable for effective 3D integrated circuits.

Introduction:

The nominal feature size of components in integrated circuit (IC) technology has decreased drastically over the last several decades producing electronics that are increasingly more advanced. However, scientists have come to realize that this nominal feature size of the components is quickly approaching both physical and quantum mechanical limits. The quantum mechanical limits arise from electrons tunneling through the thin silicon dioxide (SiO_2) insulator layer resulting in low current. The physical limits arise because the technology is approaching thin films that are a single molecule thick. To circumvent these limitations, scientists have begun researching both materials with a higher dielectric constant than SiO_2 to limit quantum tunneling, and new IC designs involving 3D fabrication of the IC components.

One promising 3D fabrication technique is the Gate-Last process which, as the name indicates, deposits the gate on the IC component last. This process requires that the fabrication temperature be less than 500°C and have an insulating layer with dielectric constant, κ, greater than 30. One material that has been investigated by many researchers for applications in future IC technology is TiO_2, because in its rutile phase its dielectric constant is over 20 times larger than SiO_2. However rutile-type TiO_2 only forms at temperatures higher than 600°C [1]. The other major polymorph of TiO_2 is the anatase structure, which forms at lower temperatures and has a dielectric constant of approximately 30 — making it an ideal material for the insulating layer of the Gate-Last process. We investigated anatase-type TiO_2 as a possible high-κ insulator for the Gate-Last process by determining its dielectric constant at three fabrication temperatures; 300, 400, and 500°C. The 500°C case was carried out previously by M. Kimura, but the results will be shown here.

We prepared TiO_2 films on SiO_2/Si samples by ALD, using tetrakis(dimethylamino)titanium (TDMAT) and water gas. These films were used to construct capacitors with structure TaC/TiO_2/SiO_2/Si with fabrication temperatures of 300, 400, and 500°C. Using these capacitors, we studied the relationship between TiO_2 thickness and fabrication temperature to determine how the fabrication temperature affected the dielectric constant of TiO_2.

Experimental:

TiO_2 thin films were deposited onto a SiO_2/Si substrate using ALD. The ALD process consisted of 50, 66, 83, and 100 cycles, where one cycle consisted of inflow of TDMAT, then argon (Ar) gas, then H_2O, and again Ar gas to purge the

Sample	Cycles	Annealing Temperature	SiO_2 Thickness ± Error	Before Annealing TiO_2 Thickness ± Error	After Annealing TiO_2 Thickness ± Error
1	100	400	4.754±0.00586	5.287±0.00491	5.317±0.00506
2	100	300	4.758±0.00603	5.205±0.00501	5.449±0.00495
3	50	400	4.734±0.00623	2.666±0.00544	2.840±0.00537
4	50	300	4.746±0.00621	2.698±0.00439	2.837±0.00581
5	83	400	4.793±0.00618	4.229±0.00503	4.355±0.00573
6	83	300	4.795±0.00635	4.214±0.00485	4.438±0.00571
7	66	400	4.821±0.00620	3.343±0.00503	3.482±0.00517
8	66	300	4.781±0.00623	3.348±0.00520	3.547±0.00520

Figure 1: Fabrication specifications and thickness results.

system before the next cycle. The substrate temperature was 200°C and the TDMAT precursor was kept at 100°C for the deposition. Post deposition annealing was done under O_2 atmosphere with flow rate of 50 sccm. The temperature was ramped at 10°C up to 300, or 400°C and held there for 30 s. The top TaC electrode of the capacitor was deposited by sputtering to a thickness of 150 nm. The samples were then annealed in a $3\%H_2/N_2$ gas to rectify any oxide ion charge.

The film thicknesses were determined by ellipsometry, and the results are shown in Figure 1. The electrical properties of the $TaC/TiO_2/SiO_2/Si$ capacitors were investigated using high-frequency capacitance-voltage (C-V) and leakage current-voltage (I-V) measurements. High-frequency C-V measurements were executed at 500 kHz and the oscillation amplitude was 30 mV. I-V measurements were performed using a step voltage sweep with a voltage step of 0.05 V. The structure of the TiO_2 films was determined previously using XRD, by M. Kimura, and is shown in Figure 2.

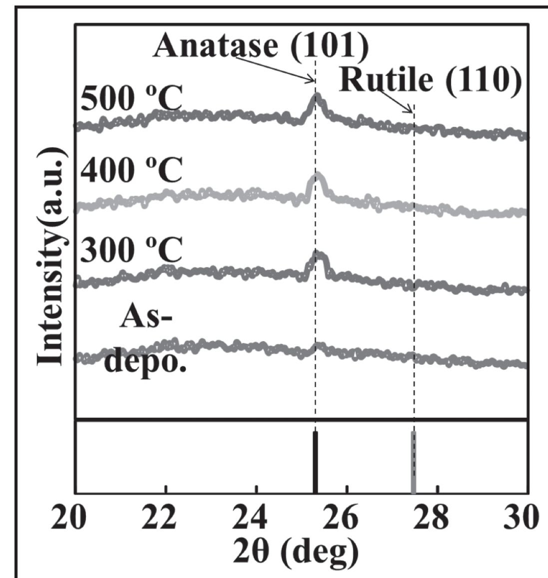

Figure 2: XRD patterns of TiO_2 films annealed at different temperatures.

Results and Discussion:

The XRD data shows how that only the anatase-type TiO_2 was deposited for all three fabrication temperature. The C-V data in Figure 3 shows that with a 500°C fabrication temperature, the dielectric constant was 34.8, at 400°C the dielectric constant was 22.8, and at 300°C the data was too inconsistent for a dielectric constant to be determined. Thus, only the 500°C fabrication process produced a TiO_2 thin film suitable for the 3D Gate-Last process.

We believe that the 300°C and 400°C fabrication temperatures were not high enough to reduce the film defects. Further research is needed to confirm this hypothesis by characterizing the film quality. We also attribute the inconsistent electrical properties of the 300°C fabrication process to poor TiO_2 film quality.

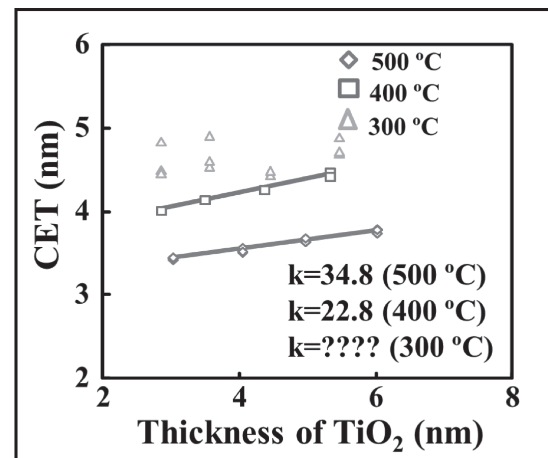

Figure 3: Capacitance Equivalent Thickness vs. Physical Thickness of TiO_2.

Conclusions:

TiO_2 thin films deposited at 500°C show promise as effective insulators for 3D fabrications, whereas the films deposited at 400°C and 300°C need to be investigated further, because of their low dielectric constant and inconsistent electrical properties. Further research is also needed to both characterize the films boundary conditions and to determine the film quality before any concrete conclusions can be made.

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References:

[1] Kadoshima, M. et al, Thin Solid Films 424 (2003) 224-228.