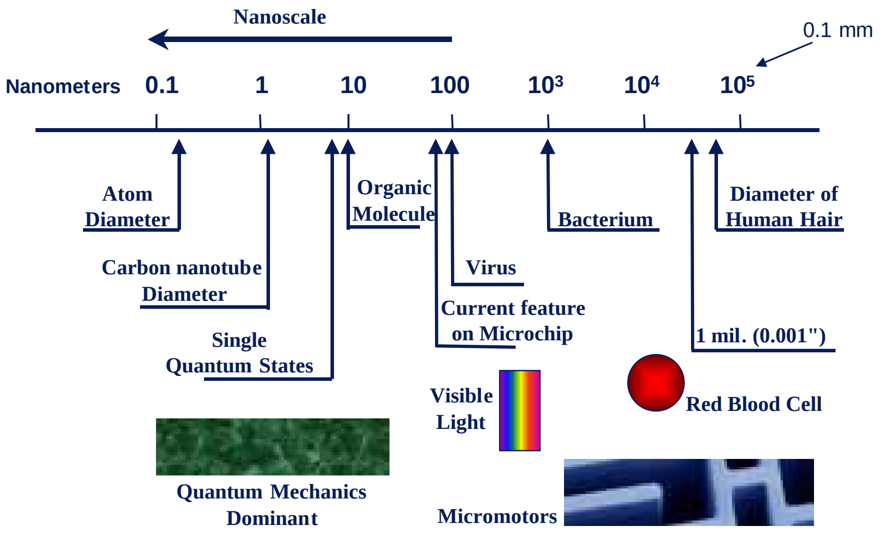
NanoCourses 2004, Section 1

Introduction
by
Sandip Tiwari

Presented by the
***CNF* Technical Staff**
for the education of CNF Users,
Potential Users, and Industrial Sponsors

Size Scales



Nanoscale

0.1 mm

Nanometers 0.1 1 10 100 10^3 10^4 10^5

Atom Diameter

Carbon nanotube Diameter

Single Quantum States

Organic Molecule

Virus

Current feature on Microchip

Bacterium

Diameter of Human Hair

1 mil. (0.001")

Visible Light

Red Blood Cell

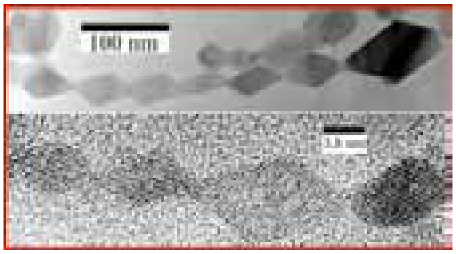
Quantum Mechanics Dominant

Micromotors

Why nano now?

Is Nanotechnology Something New?

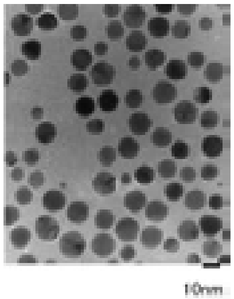
- Materials with nanoscale components are widespread



Is Nanotechnology Something New?

- Humans **have been** making **systems with** nanoscale components **for thousands of years**
- **We have been** *engineering* **materials at the nanoscale for many years.**

stained glass



nanoscale gold particles
in glass give red color

So Why All of the Excitement?

Why Now?

Tools for seeing and manipulating structures on nanometer scales have been developed in the last 10-20 years.

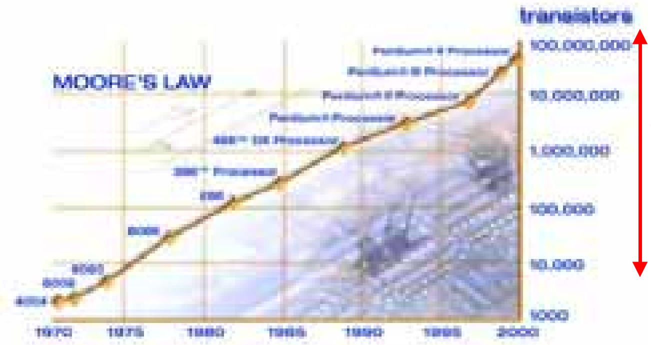
Once you can see what you are doing and make changes, you can begin to do interesting work.

Why Nano?

New scientific opportunities: An unexplored world, new properties to understand.

→ **New technologies:**
electronics, computer memory, bio-technology, nano-mechanical devices, new materials, other applications

Information Processing



100,000 times improvement!

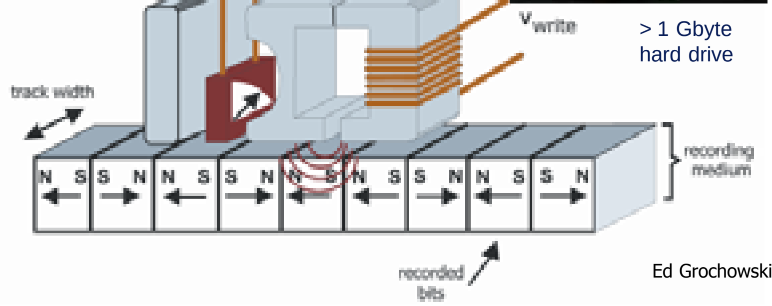
Predictions

Pentium 5 linewidth = 90 nm

Magnetic Recording

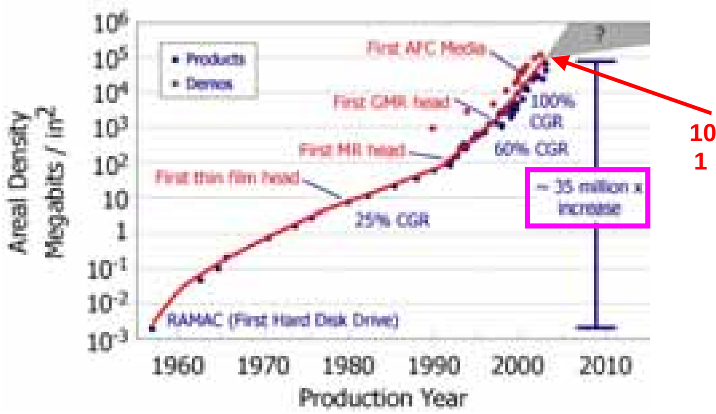
- Three core magnetic components
  - media
  - writer
  - reader
- All require nanoscale engineering today

> 1 Gbyte hard drive



Ed Grochowski

Information Storage

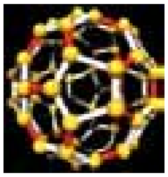


100 Gbits/in^2=
1 bit/(80 nm)^2

Ed Grochowski

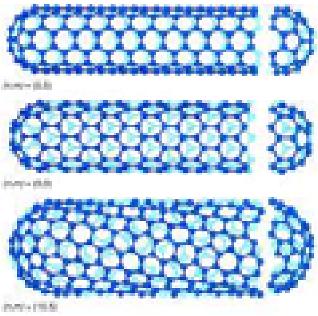
Why the NNI now?

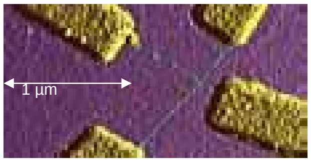
- New discoveries, naturally nanoscale materials



Buckyball

Carbon
nanotubes





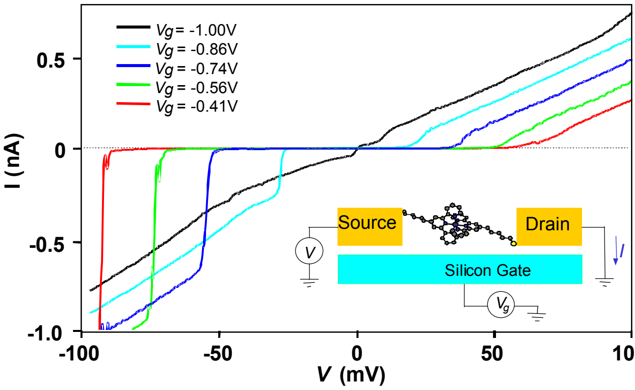
Carbon Nanotube - single carbon molecule

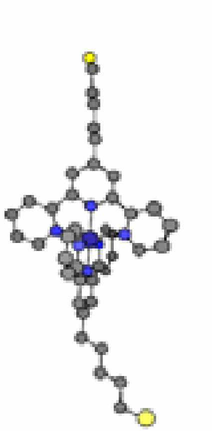
Either metallic or semiconducting, depending on the pattern of rolling

Better thermal conductor than any other material

Stronger than any other material

Single Atom/Molecule Transistor



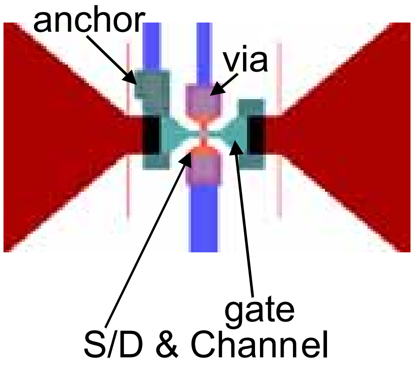


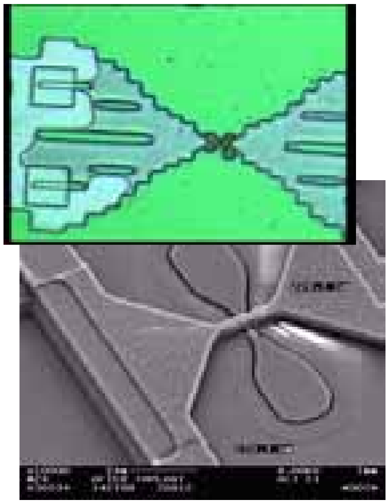
- The single molecule works as a transistor, but
  - Slow
  - Works only at low temperatures, not room temperature
  - No Gain

Park, McEuen, Ralph, Abruna et al.

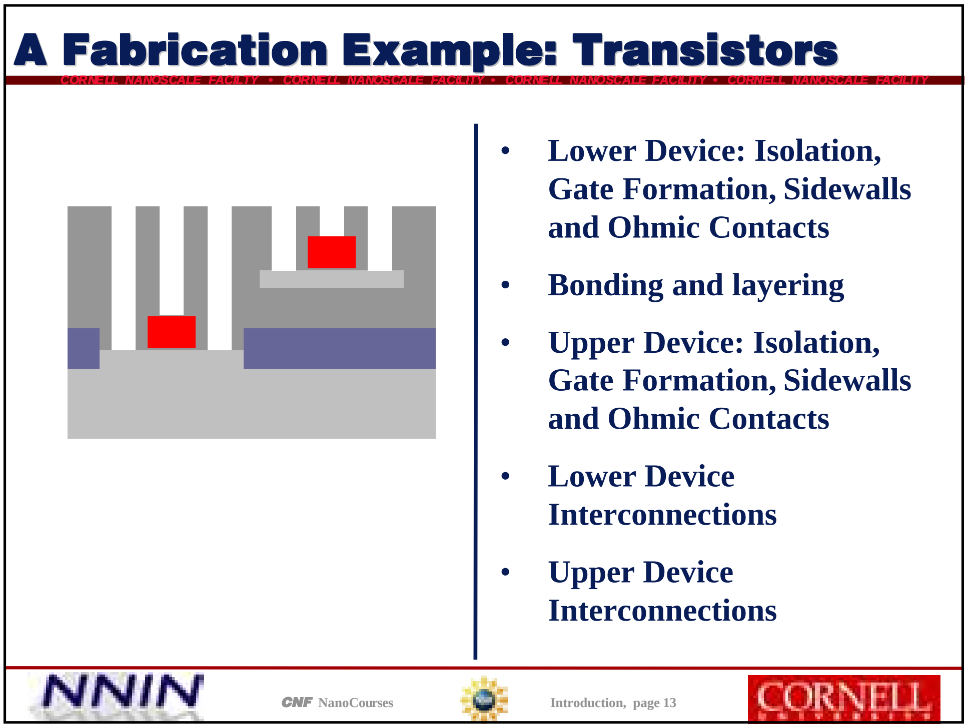
- Now at the stage of very basic research, not close to useful technology.

Interdisciplinary: Electronic-Microfluidic



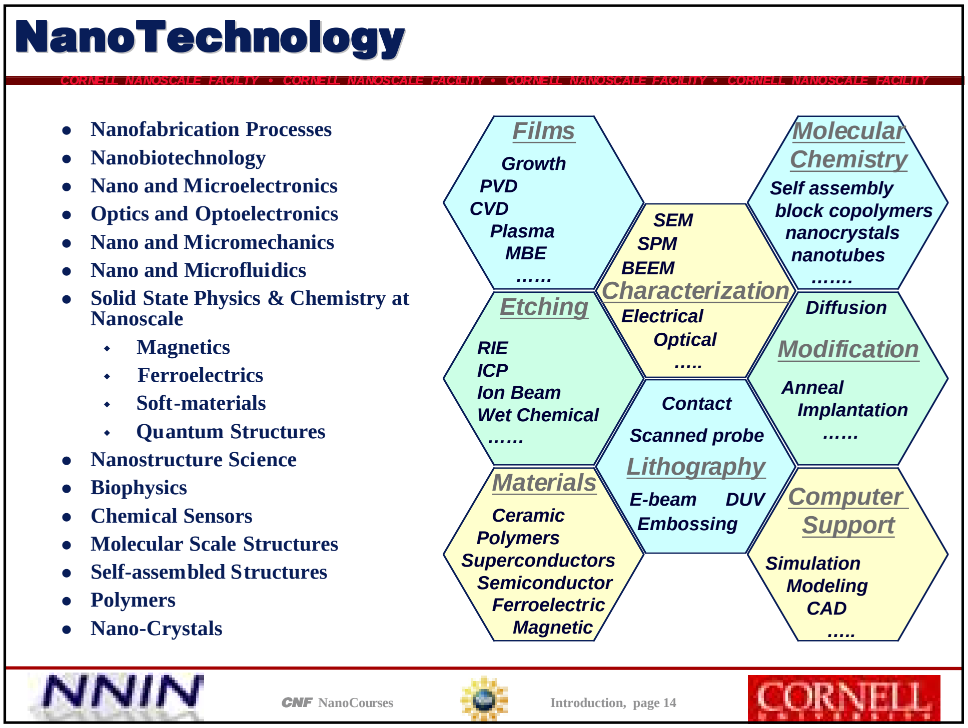


- A. Gokirmak & S. Tiwari (CNF)



A Fabrication Example: Transistors

- Lower Device: Isolation, Gate Formation, Sidewalls and Ohmic Contacts
- Bonding and layering
- Upper Device: Isolation, Gate Formation, Sidewalls and Ohmic Contacts
- Lower Device Interconnections
- Upper Device Interconnections



NanoTechnology

- Nanofabrication Processes
- Nanobiotechnology
- Nano and Microelectronics
- Optics and Optoelectronics
- Nano and Micromechanics
- Nano and Microfluidics
- Solid State Physics & Chemistry at Nanoscale
  - Magnetics
  - Ferroelectrics
  - Soft-materials
  - Quantum Structures
- Nanostructure Science
- Biophysics
- Chemical Sensors
- Molecular Scale Structures
- Self-assembled Structures
- Polymers
- Nano-Crystals

Films
Growth
PVD
CVD
Plasma
MBE
……

Molecular Chemistry
Self assembly
block copolymers
nanocrystals
nanotubes
…….

SEM
SPM
BEEM
Characterization
Electrical
Optical
…..

Etching
RIE
ICP
Ion Beam
Wet Chemical
……

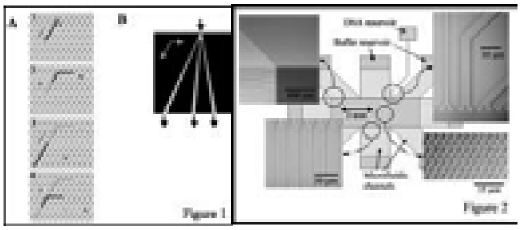
Diffusion
Modification
Anneal
Implantation
……

Contact
Scanned probe
Lithography
E-beam DUV
Embossing

Materials
Ceramic
Polymers
Superconductors
Semiconductor
Ferroelectric
Magnetic

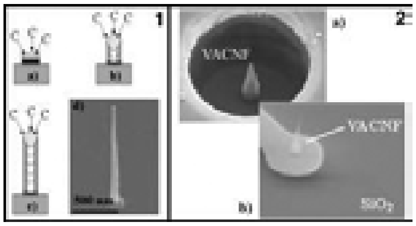
Computer Support
Simulation
Modeling
CAD
…..

Wide Array of Applications

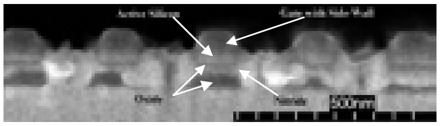


Fractionating Prism: Continuous Sorting, Austin et al.
http://www.cnf.cornell.edu/nnun/2002NNUNreports.html

RoboRat: http://www.washingtonpost.com/ wp-dyn/articles/A18261-2002May1.html)



Field-Emission Displays, Simpson et al.
http://www.cnf.cornell.edu/nnun/2002NNUNreports.html



Smallest Non-volatile Memories
H. Silva et al. IEEE Trans. on Nano. (2004)

Is it all hype, or is it real?

NANOTECH REPORT
60 Fifth Avenue • New York, NY 10011

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"I know with absolute certainty that nanotechnology WILL change the world in ways it is still difficult to imagine!

"For the long-term investor it represents a greater opportunity for profits than even the PC revolution.

"WARNING: its future is so incredible, it opens the door to a new wave of Wall Street over-hype."

STEVE FORBES

Here's how to keep your feet planted firmly in the real world... and your portfolio filled with long-term nanotech winners in the most astonishing and far-reaching revolution yet.

HALF-PRICE OFFER!

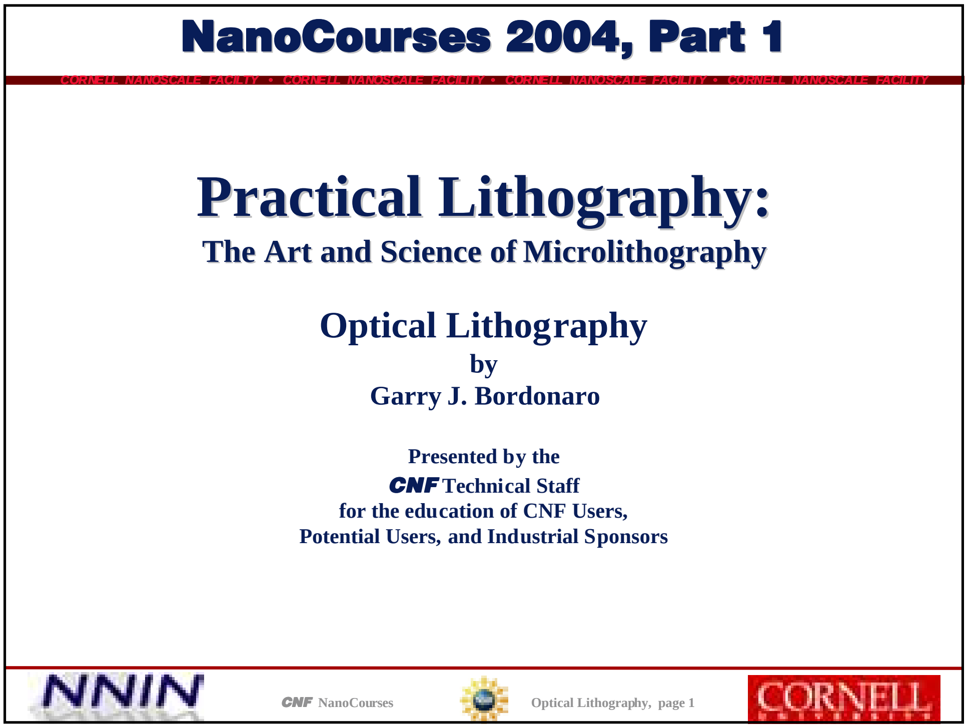
Plus 2 FREE Reports!

All-New Investment Advisory from Forbes

A Caution

Nanotechnology is big, but
do not believe everything you read or
see in popular press.

Be perceptive, use your knowledge and
critical thinking.



NanoCourses 2004, Part 1

Practical Lithography:

The Art and Science of Microlithography

Optical Lithography

by
Garry J. Bordonaro

Presented by the
CNF Technical Staff
for the education of CNF Users,
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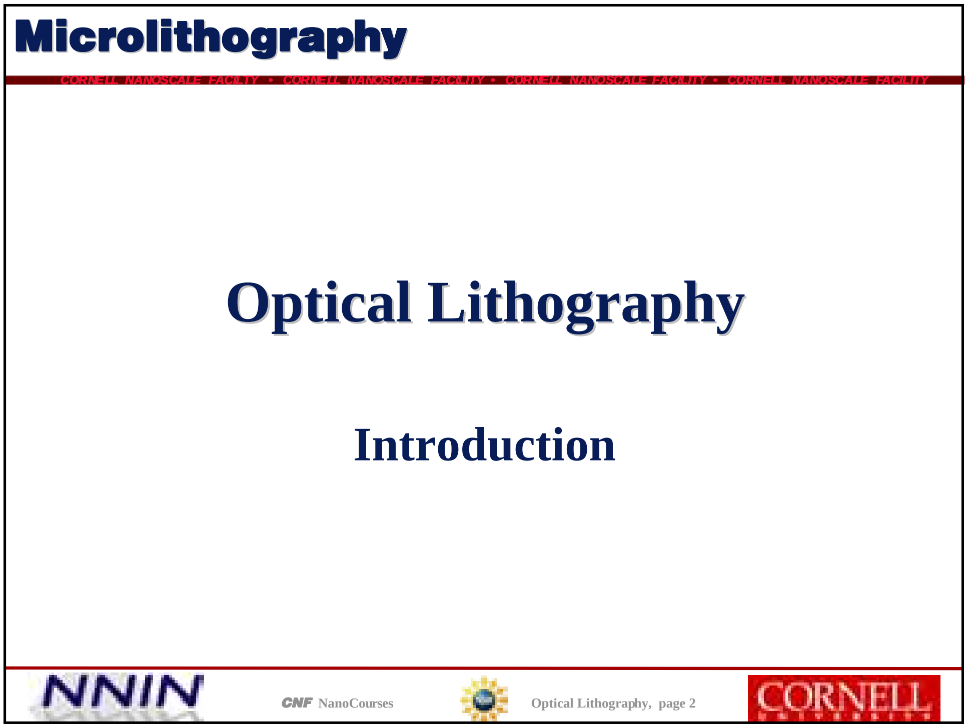


Microlithography

Optical Lithography

Introduction

Introduction

- Optical Lithography - Mask Making
- Optical Lithography - Exposure Tool
- Optical Lithography - Techniques
- Pattern Design (CAD)

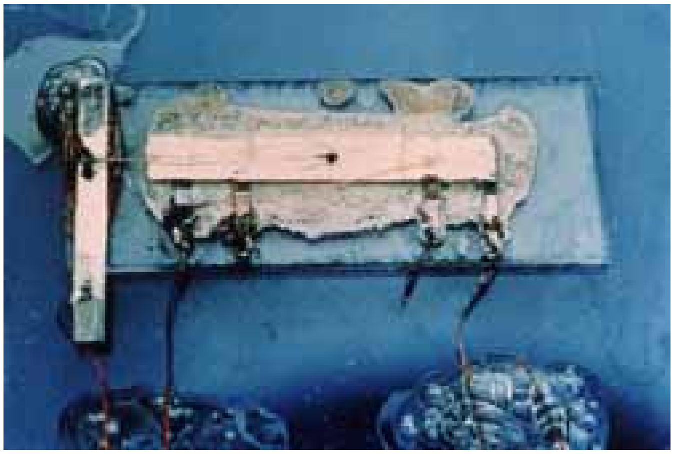
A Brief History

- The first transistor - 1947 at Bell Labs by researchers Bardeen, Brattain, and Shockley
- The first integrated circuit - 1959 at Texas Instruments by Jack Kilby.
- 1959 - Fairchild Camera, Robert Noyce - planar technology, and silicon dioxide as an insulating material on a silicon substrate.

First Transistor – Bell Labs 1947

Courtesy Lucent Technolgies

First Integrated Circuit – Texas Instruments 1959



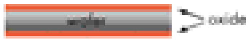
Courtesy of Texas Instruments

Industry Foundation – The Silicon Wafer

Courtesy Intel

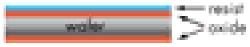
Semiconductor Processing

Diffusion



A layer of material such as oxide or polysilicon is grown from or deposited onto the wafer. The first material deposited helps create the first layer of the semiconductor "skyscraper."

Coat-Bake

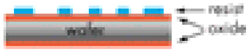


The photo resist, a light sensitive protective layer, is applied. The liquid photo resist is then baked to form a hardened layer that is light sensitive but resistant to chemical attack. This hardened layer acts much like the film in a camera and is used to transfer circuit images to the wafer.

Align

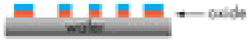
A reticle with the circuit pattern for a given level is aligned over the wafer. Ultraviolet light shines through the clear portions of the reticle exposing the pattern onto the photosensitive resist.

Develop



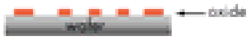
The photo resist is chemically treated in a develop process that selectively removes the exposed regions of resist and leaves the unexposed regions containing the pattern information on the reticle.

Dry Etch



The wafers are placed in a vacuum chamber, and a mixture of gases are pumped in and excited by electricity. This plasma eats away the material not protected by the remaining resist. When the unprotected material has been removed, the remaining material begins the pattern of the circuitry.

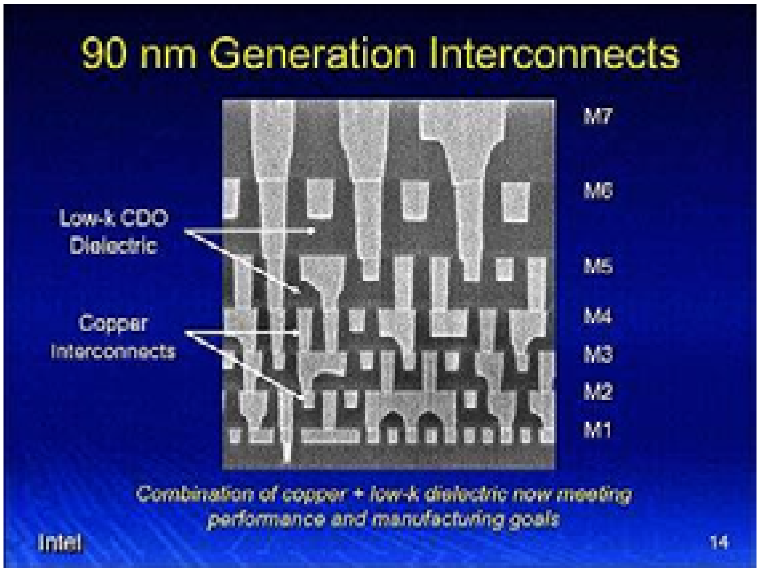
Wet Etch & Clean



The remaining resist is removed in wet etch to reveal the patterned oxide layer. Then the wafer is cleaned. The process is repeated up to 18 times to create the various layers necessary for each part's circuitry.

Micron Technology

State-of-the-Art Manufacturing

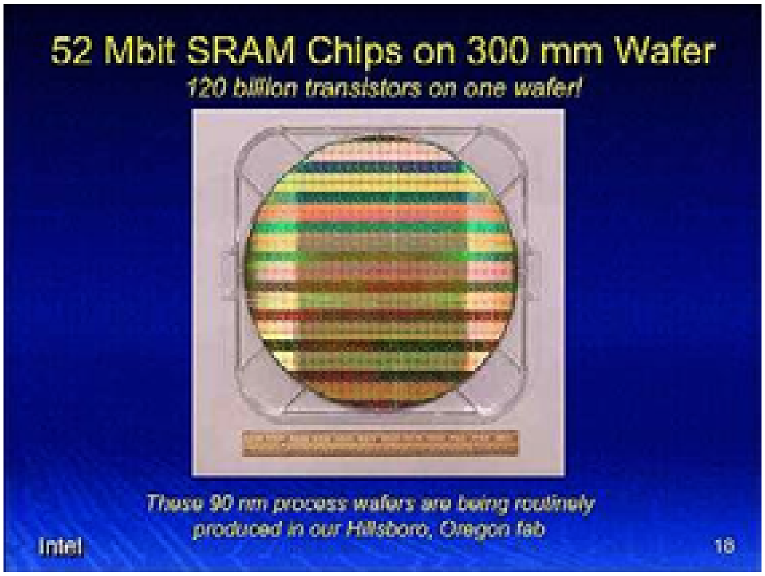


90 nm Generation Interconnects

Combination of copper + low-k dielectric now meeting performance and manufacturing goals

Intel

State-of-the-Art Manufacturing



52 Mbit SRAM Chips on 300 mm Wafer

120 billion transistors on one wafer!

These 90 nm process wafers are being routinely produced in our Hillsboro, Oregon fab

Intel

IBM East Fishkill Wafer Fab

Courtesy IBM

Market-Driven Technology

GeForce 6800

Revolutionary performance & complete Shader Model 3.0

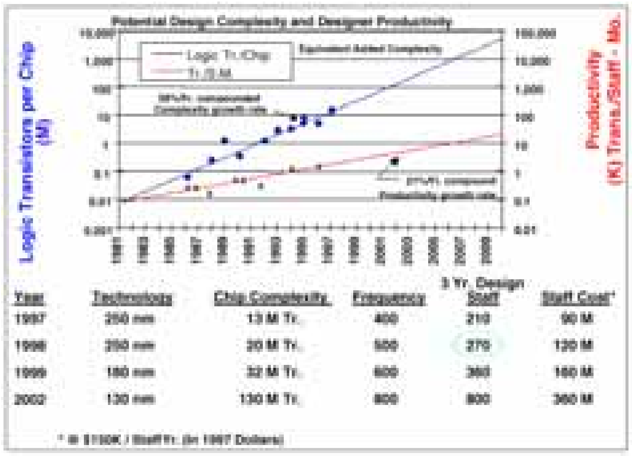
- Complete Native Shader Model 3.0 Support
  - Full support for shader model 3.0
  - Vertex Texture Fetch / Long programs / Pixel Shader flow control
  - Full speed fp32 shading
- OpenEXR High Dynamic Range Rendering
  - Floating point frame buffer blending
  - Floating point texture filtering
- Unparalleled Performance
  - 222M xtors / 0.13um @ IBM
  - 6 vertex units / 16 pixel pipelines
- Next Generation Video
  - VMR / High quality compositing
  - Hardware MPEG encode / decode
  - HDTV Output
- PCI Express

Personal Computer Products

Intel Xeon

IBM Power PC

Increasing Device Density



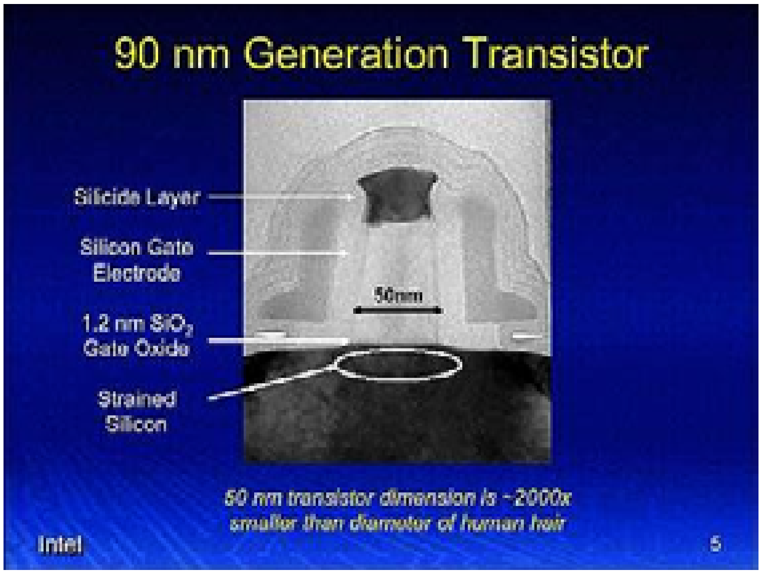
Year	Technology	Chip Complexity	Frequency	3 Yr. Design Staff	Staff Cost*
1997	250 nm	13 M Tr.	400	210	90 M
1998	250 nm	20 M Tr.	500	270	120 M
1999	180 nm	32 M Tr.	600	360	160 M
2002	130 nm	130 M Tr.	800	800	360 M

* @ $150K / Staff Yr. (In 1997 Dollars)

Figure 5 The Design Productivity Gap

SIA Roadmap

Leading-Edge Processes



90 nm Generation Transistor

50 nm transistor dimension is ~2000x smaller than diameter of human hair

Intel

Semiconductor Processing

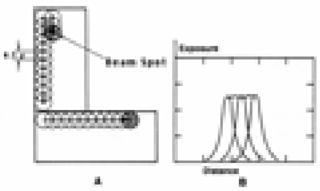
- Manufacture of devices depends on selective processes:
  - Removal of material -- Etching
  - Addition of material -- Deposition
  - Modification of material -- Implantation, diffusion, etc.

Types of Exposure

- Light -- 436 nm - 157 nm; near UV to Deep UV optical lithography
- X-rays -- 13 nm - 0.4 nm; x-ray lithography
- Electrons -- 10 keV - 100 keV; electron beam lithography
- Ions -- 50 keV - 200 keV; focused ion beam lithography

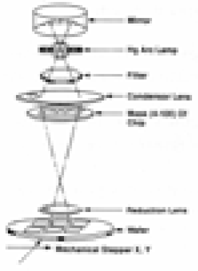
Exposure Methods

E-beam Dose Pattern



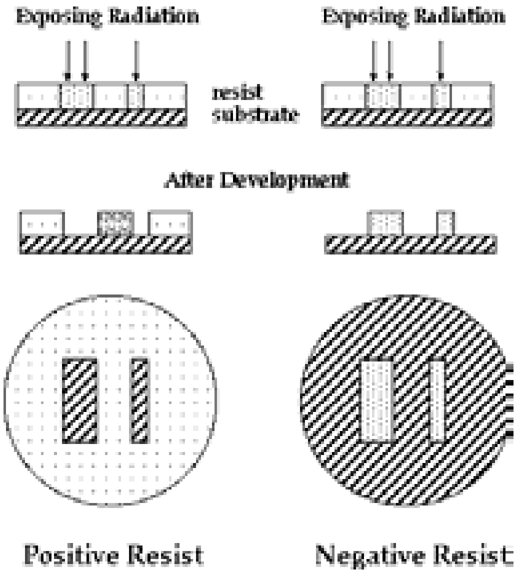
W. Moreau, Semiconductor Lithography, Plenum, New York, 1988, p. 423.

Stepper Optics

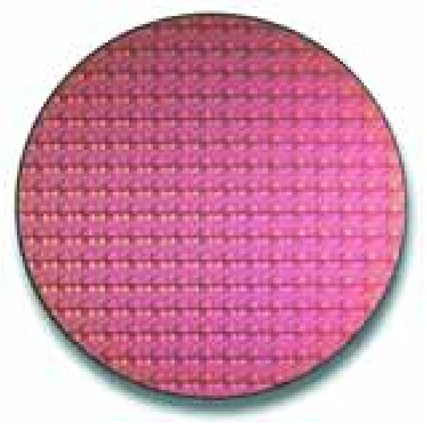


W. Moreau, Semiconductor Lithography, Plenum, New York, 1988, p. 363.

Resist Development

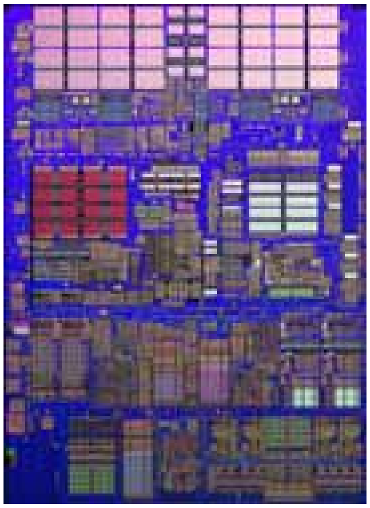


300mm of Silicon Wafer (12")



Intel 300mm Wafers

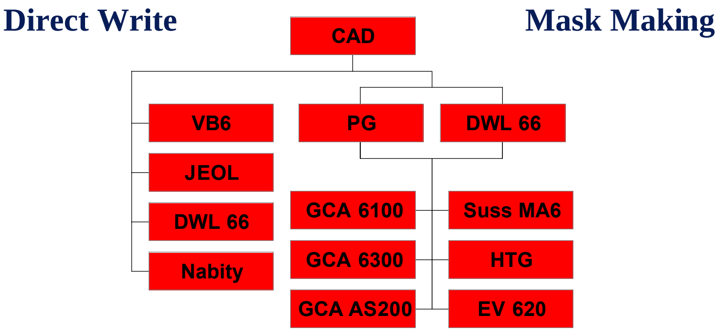
Finished Processor Die



IBM Power PC

Intel Pentium 4

Lithography at CNF



Your Pattern Requirements

- **Considerations:**
  - **The requirements of the lithography tool**
  - **The requirements of the technique you will use for the pattern transfer**

Starting Suggestions

- **Think** about what type of design you want and how to implement it.
- **Gather information** from the course notes, staff members, and other students about the best tools and techniques to use before you actually sit down and design the pattern.
- **Design the pattern** using the information you have gathered paying careful attention to the requirements listed above.
- **Perform** lithography, pattern transfer, etc.
- **Repeat steps 1 - 4** as many times as necessary to get it right.

To Aid the Staff (and you)

- The more thinking and preparation you do, the more intelligent the questions you ask, and the more time you end up saving the staff member.
- The more advance notice you can give about when you would like to talk about your process or be trained on equipment, the better.
- The more responsible you can be around the lab, the less we have to clean up after you, and the more time we have for answering your questions.
- **And, last but not least, please be patient!**

Microlithography

Optical Lithography

Mask Making

Pattern Generators

Heidelberg DWL 66

GCA/Mann 3600F

GCA/Mann 3600F Specifications

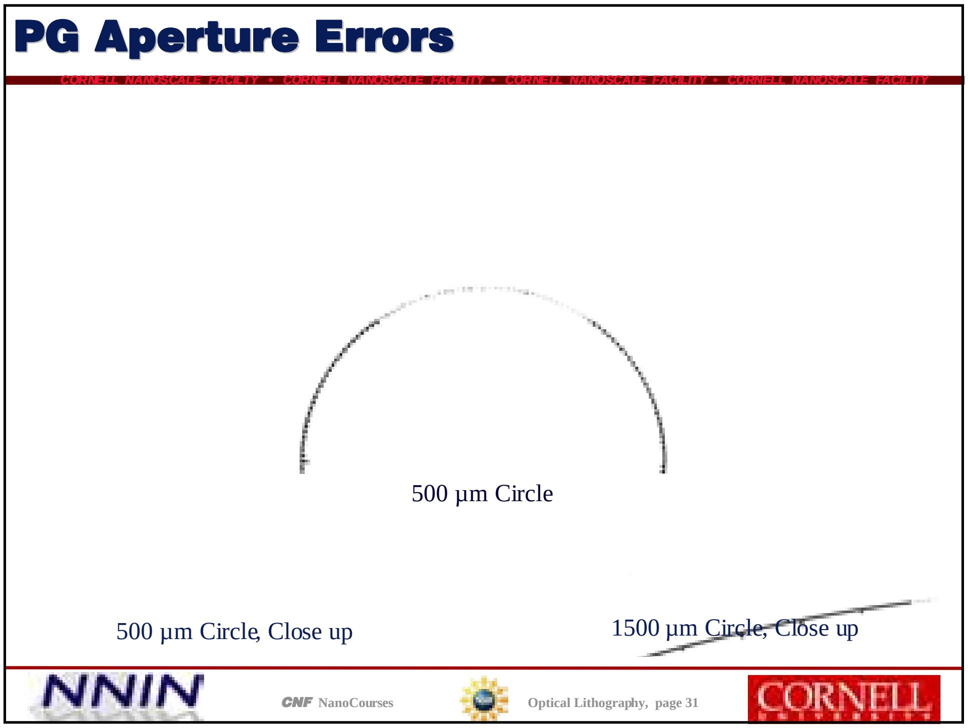
- Data input: 0.1 µm; this is the least count for object placement
- Aperture: 2 µm - 1500 µm in 0.5µm increments
- Rotation: 0 - 89.9° in 0.1° increments
- Image positioning accuracy: ± 0.6 µm over 150 mm of stage motion -- this is 4 ppm
- Aperture error:
  - ± 0.35 µm from 2 µm - 125 µm
  - ± 0.3 % from 125 µm - 425 µm
  - ± 1.25 µm from 425 µm - 1500 µm

Heidelberg DWL66 Specifications

- **Data input: 0.01 µm; this is the least count for object placement**
- **Spot size: 0.6 µm with 2 mm lens; 2 µm with 10 mm lens**
- **Stage motion range: 200 mm**
- **Image positioning accuracy: ± 0.05 µm over 100 mm of stage motion -- this is 0.5 ppm**
- **Alignment error: +/- 100 nm**

PG Aperture and Positioning Errors

Contact (1:1)	2.0 μm	2.0 μm	17.5 %
Stepper (5:1)	5.0 μm	1.0 μm	7.0 %
Stepper (10:1)	6.0 μm	0.6 μm	5.0 %



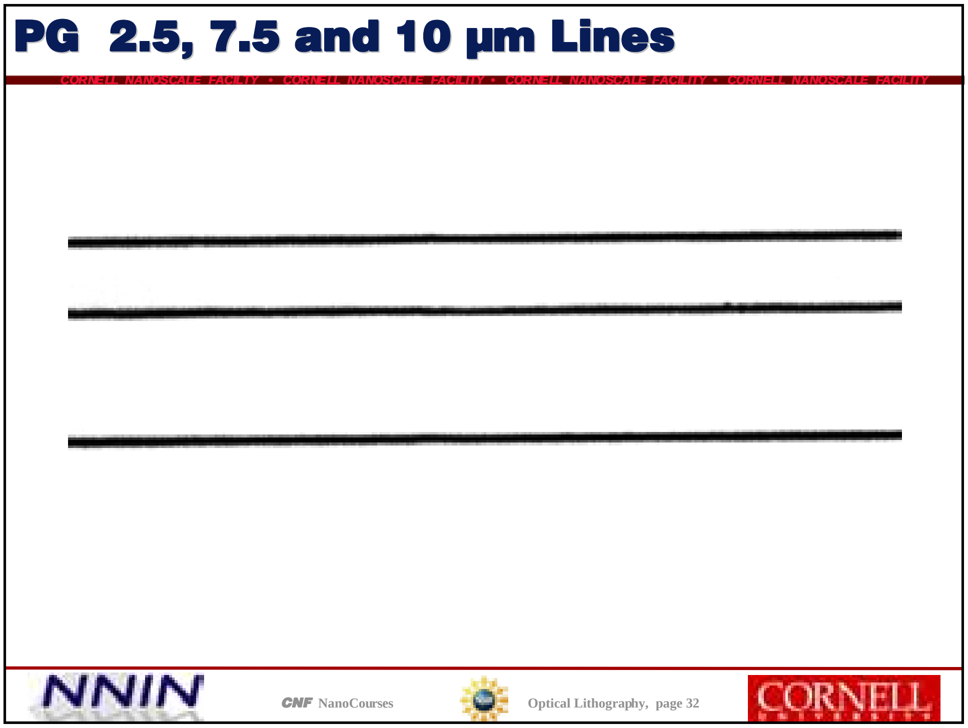
PG Aperture Errors

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

500 µm Circle

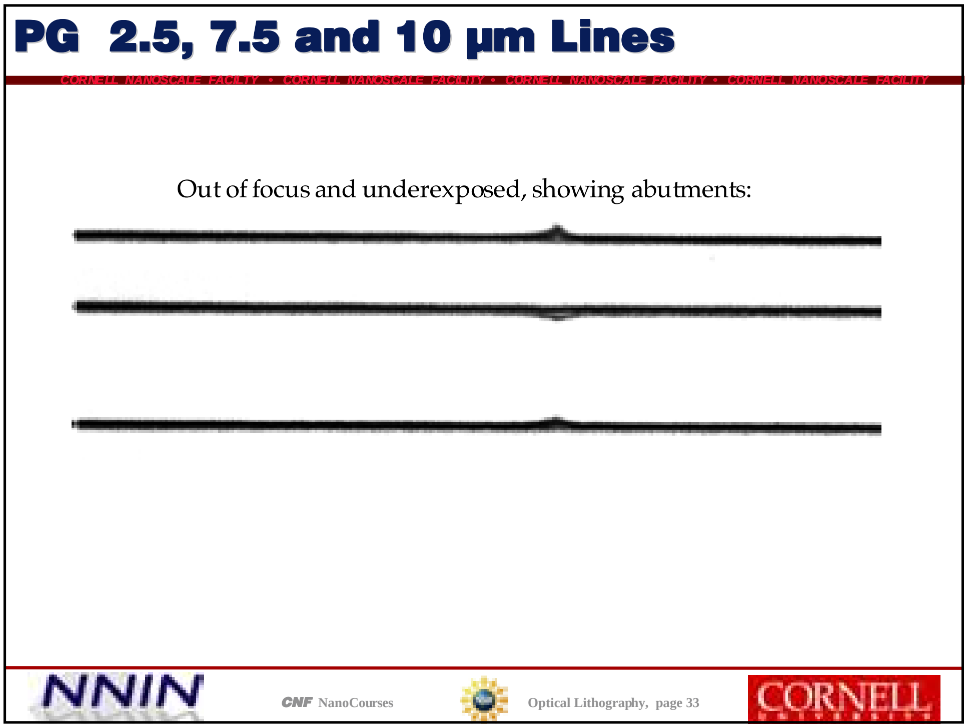
500 µm Circle, Close up

1500 µm Circle, Close up



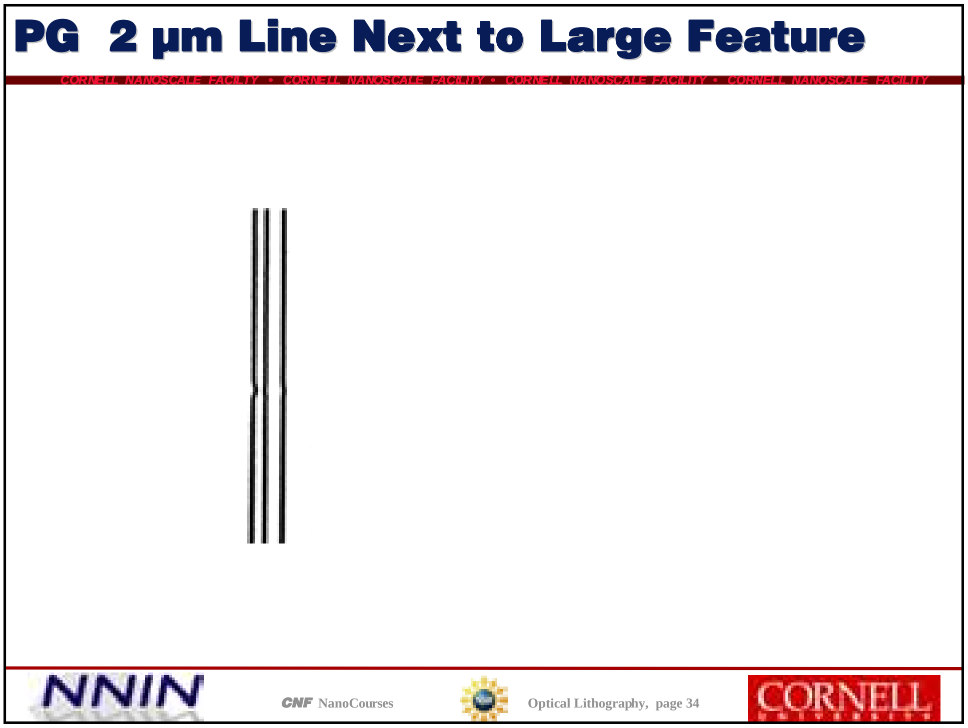
PG 2.5, 7.5 and 10 µm Lines

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

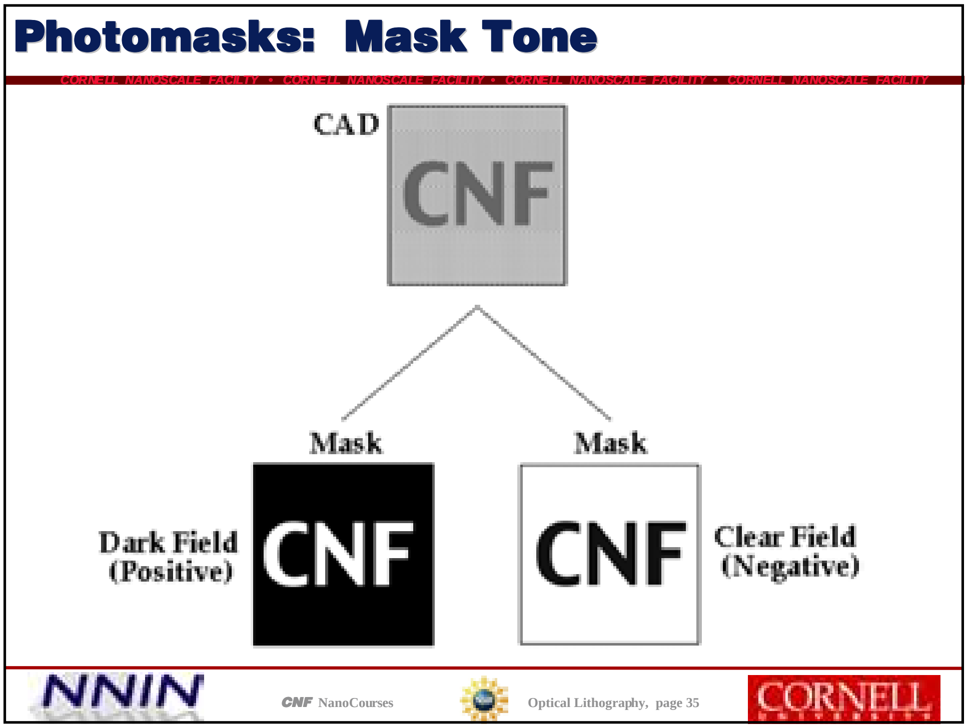


PG 2.5, 7.5 and 10 µm Lines

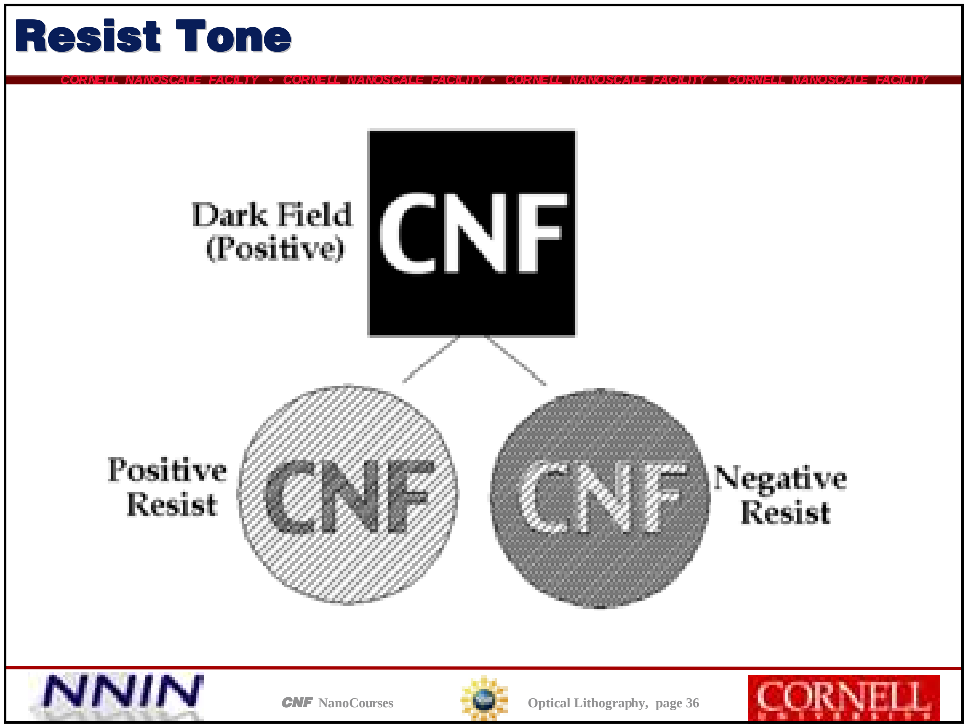
Out of focus and underexposed, showing abutments:



PG 2 µm Line Next to Large Feature

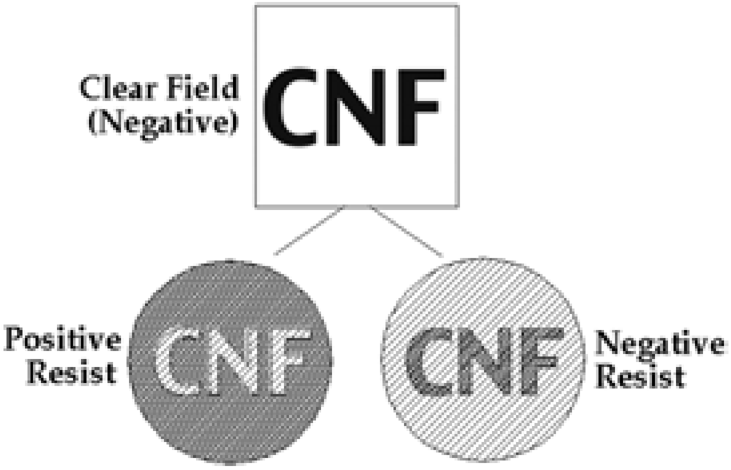


Photomasks: Mask Tone



Resist Tone

Resist Tone

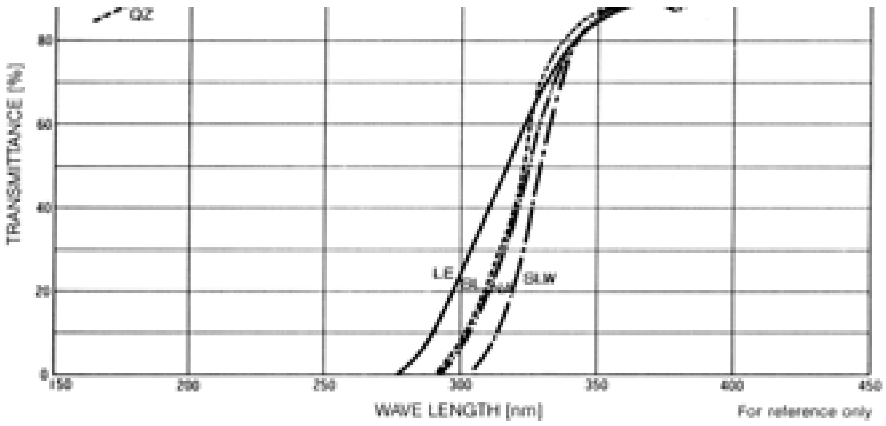


Types of Glass

- **Thermal coefficients for different types of glass:**

Soda-lime:	**9.3 ppm/ºC**
Borosilicate:	**3.7 ppm/ºC**
Quartz:	**0.5 ppm/ºC**

Transmission Properties



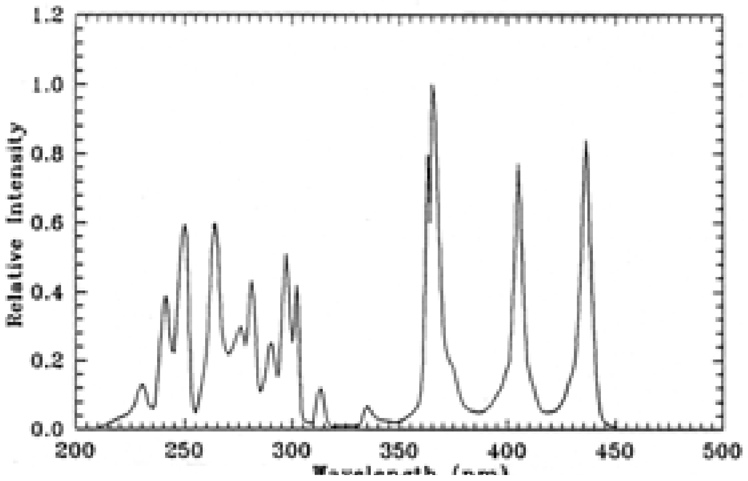
Other Mask-making Techniques

- E-beam Direct-write
- GCA/Mann 6300 in Photorepeater Mode
- Outside vendors

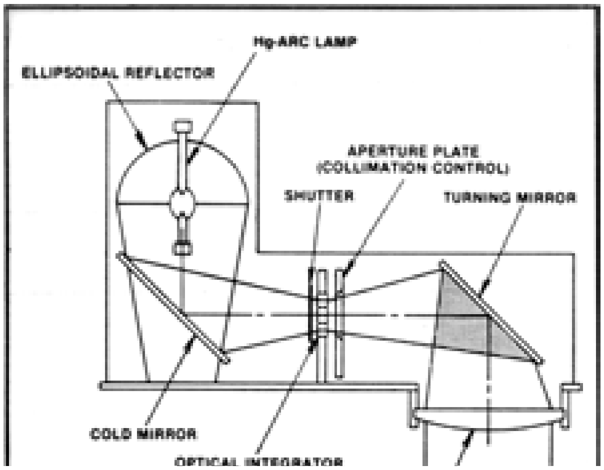
Optical Lithography:

Exposure Tools

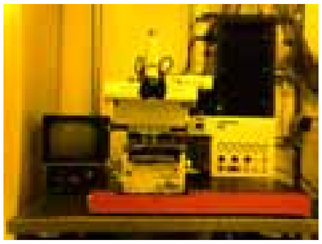
Hg UV Lamp Spectrum



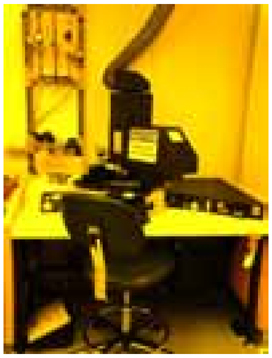
Contact Aligner



Contact Mask Aligners

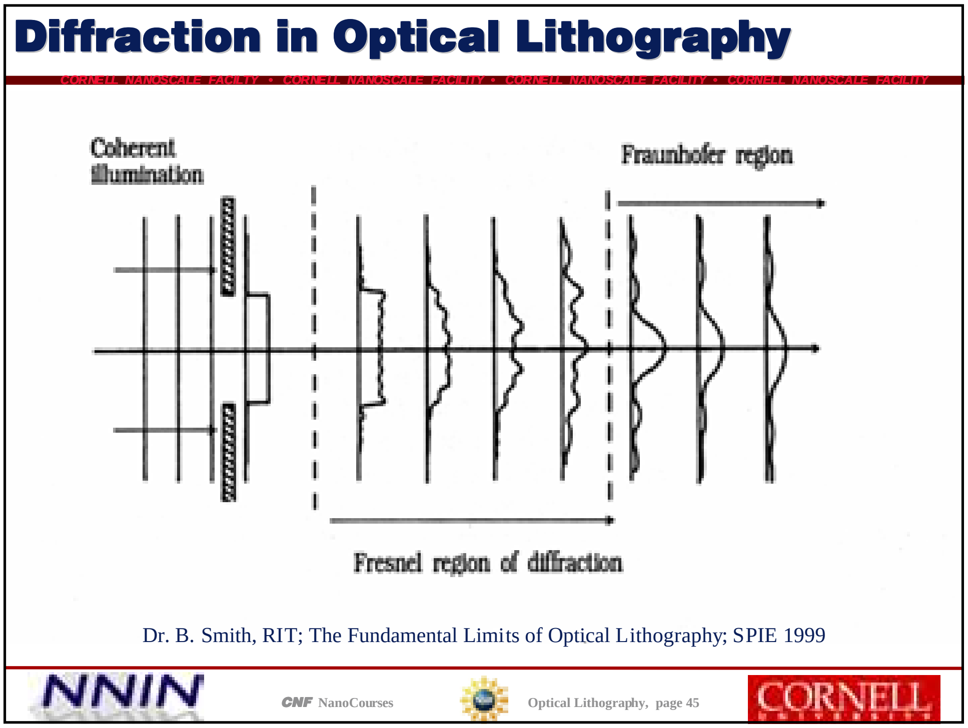


Karl Suss
MA6



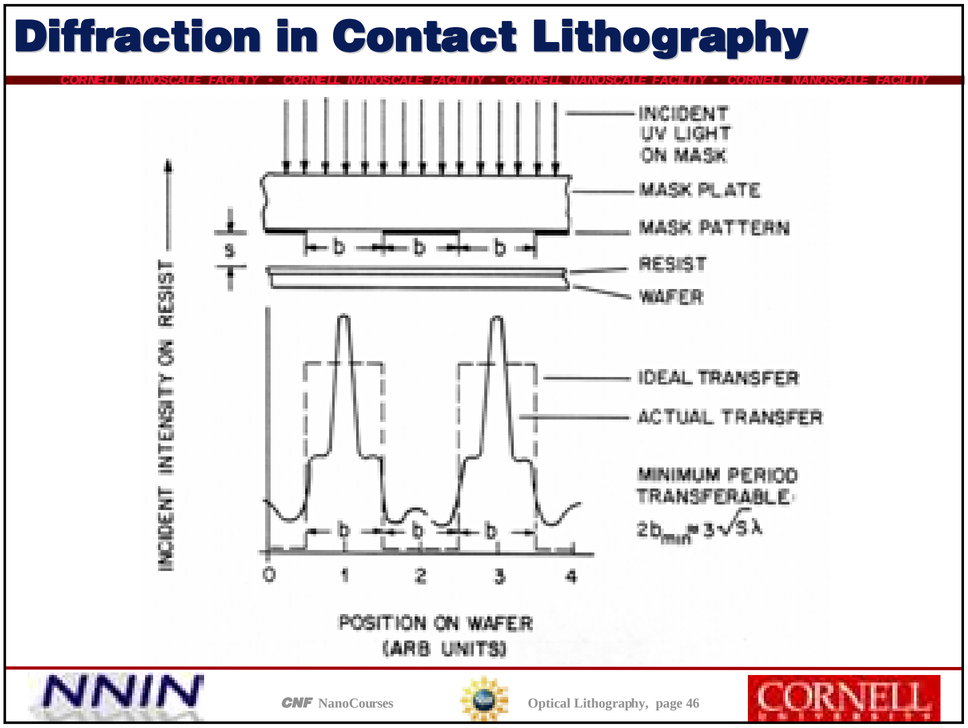
HTG 3HR

EVG 620



Diffraction in Optical Lithography

Dr. B. Smith, RIT; The Fundamental Limits of Optical Lithography; SPIE 1999

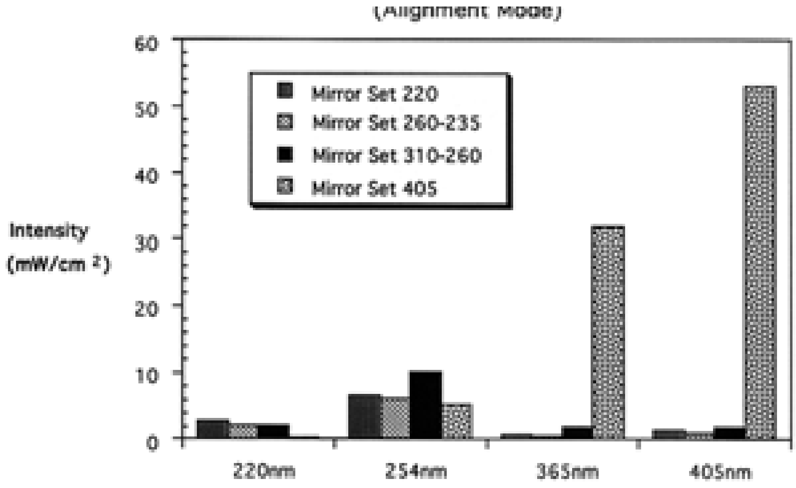


Diffraction in Contact Lithography

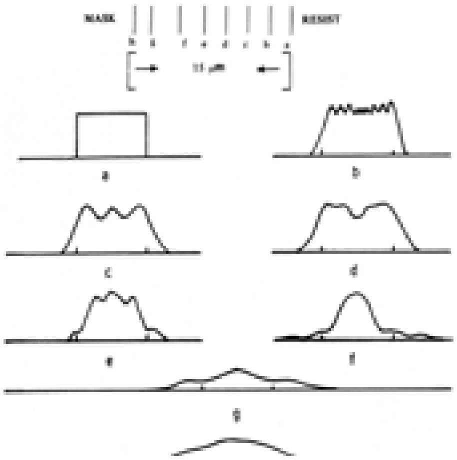
Resolution in Contact Lithography

$$2\,b_{min} = 3\,[\lambda\, d\ /\ 2\,]^{1/2}$$

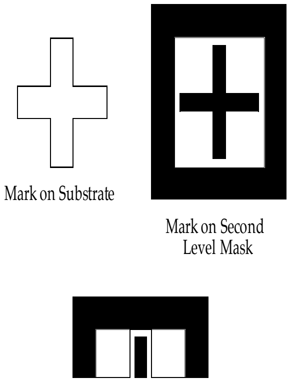
HTG Aligner Output Spectrum

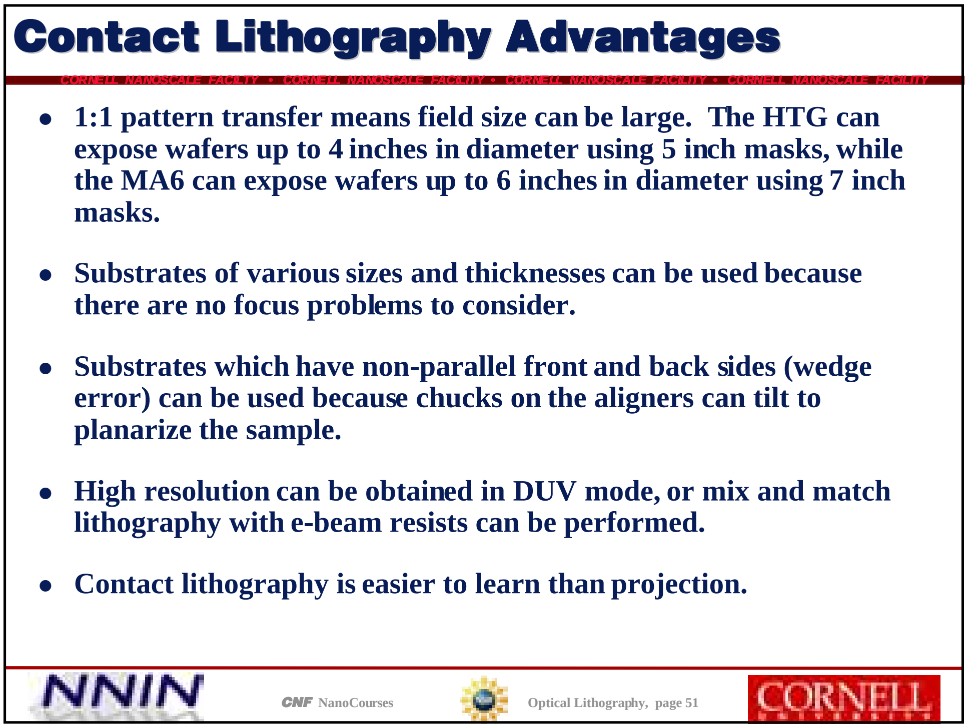


Contact Aligner Diffraction



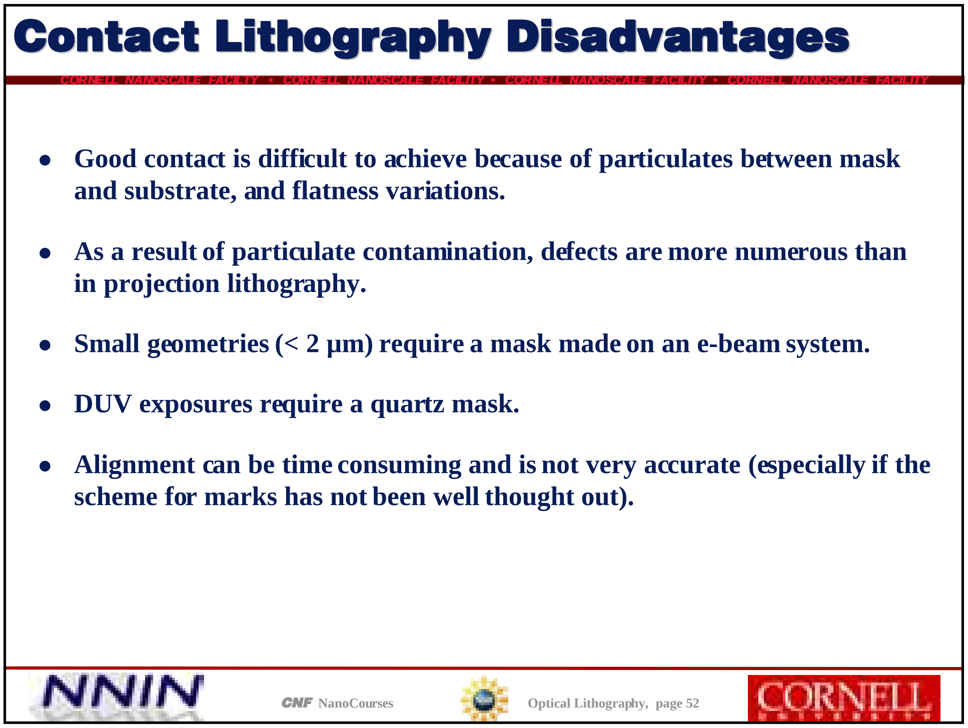
Contact Alignment Marks





Contact Lithography Advantages

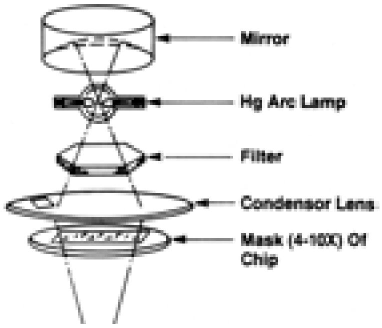
- 1:1 pattern transfer means field size can be large. The HTG can expose wafers up to 4 inches in diameter using 5 inch masks, while the MA6 can expose wafers up to 6 inches in diameter using 7 inch masks.
- Substrates of various sizes and thicknesses can be used because there are no focus problems to consider.
- Substrates which have non-parallel front and back sides (wedge error) can be used because chucks on the aligners can tilt to planarize the sample.
- High resolution can be obtained in DUV mode, or mix and match lithography with e-beam resists can be performed.
- Contact lithography is easier to learn than projection.



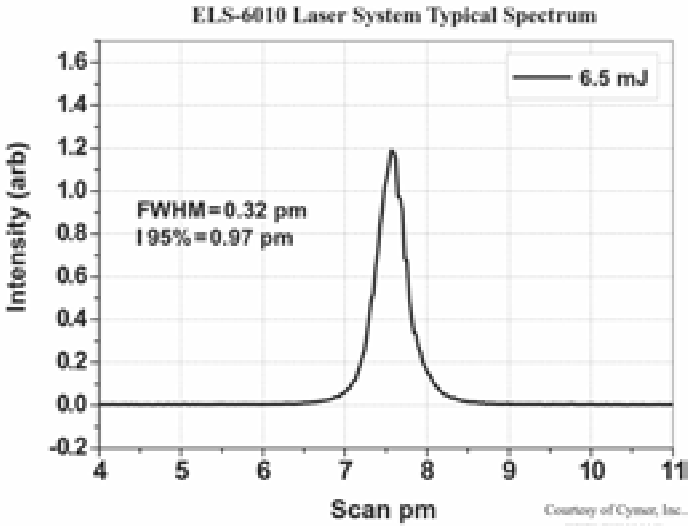
Contact Lithography Disadvantages

- Good contact is difficult to achieve because of particulates between mask and substrate, and flatness variations.
- As a result of particulate contamination, defects are more numerous than in projection lithography.
- Small geometries (< 2 µm) require a mask made on an e-beam system.
- DUV exposures require a quartz mask.
- Alignment can be time consuming and is not very accurate (especially if the scheme for marks has not been well thought out).

Stepper Optics

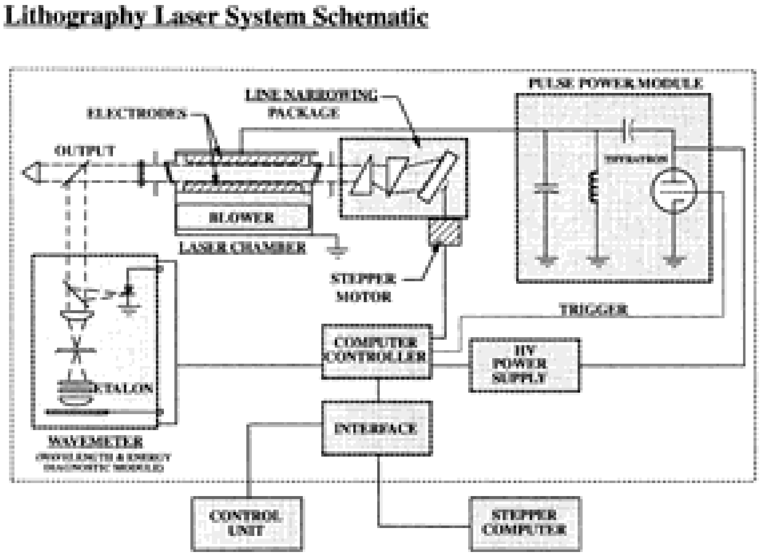


248nm Excimer Laser Spectrum



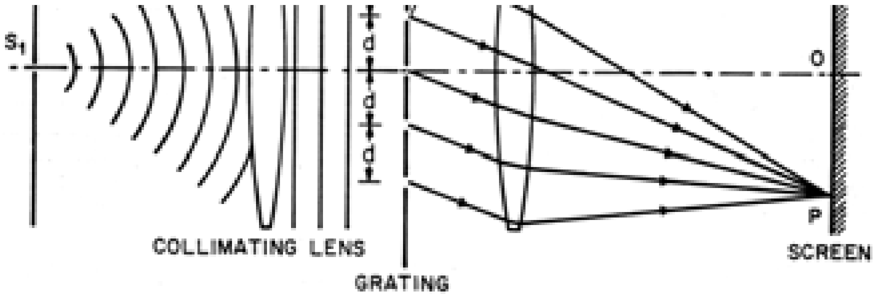
Courtesy of Cymer, Inc.
www.cymer.com

Excimer Laser Schematic

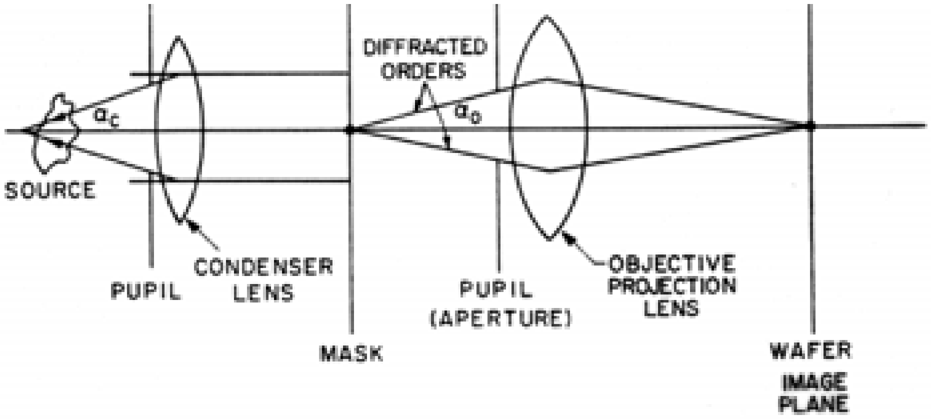


Stepper Diffraction

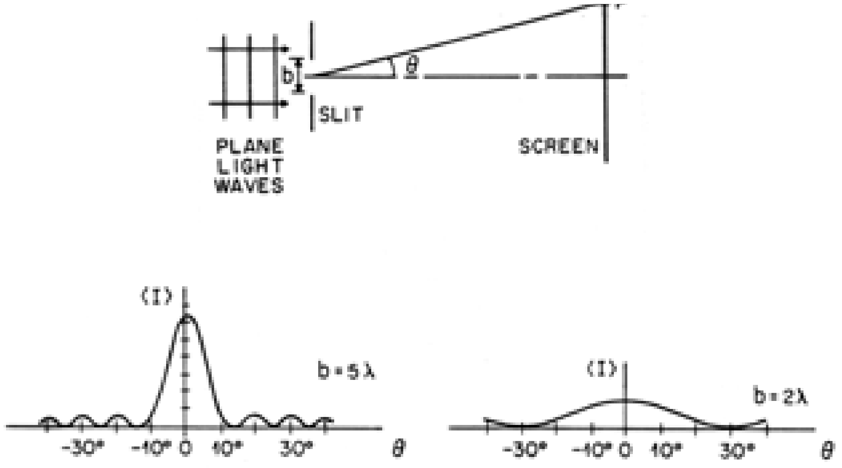
$$\sin \theta = N \lambda / d$$

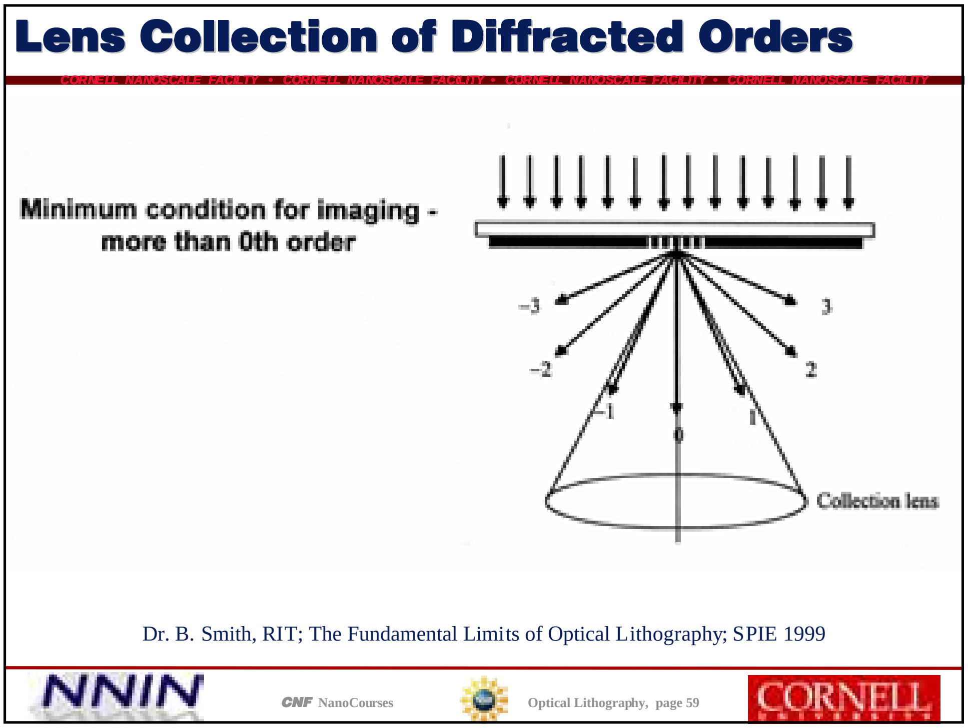


Diffraction in a Grating



Diffracted Order Spread

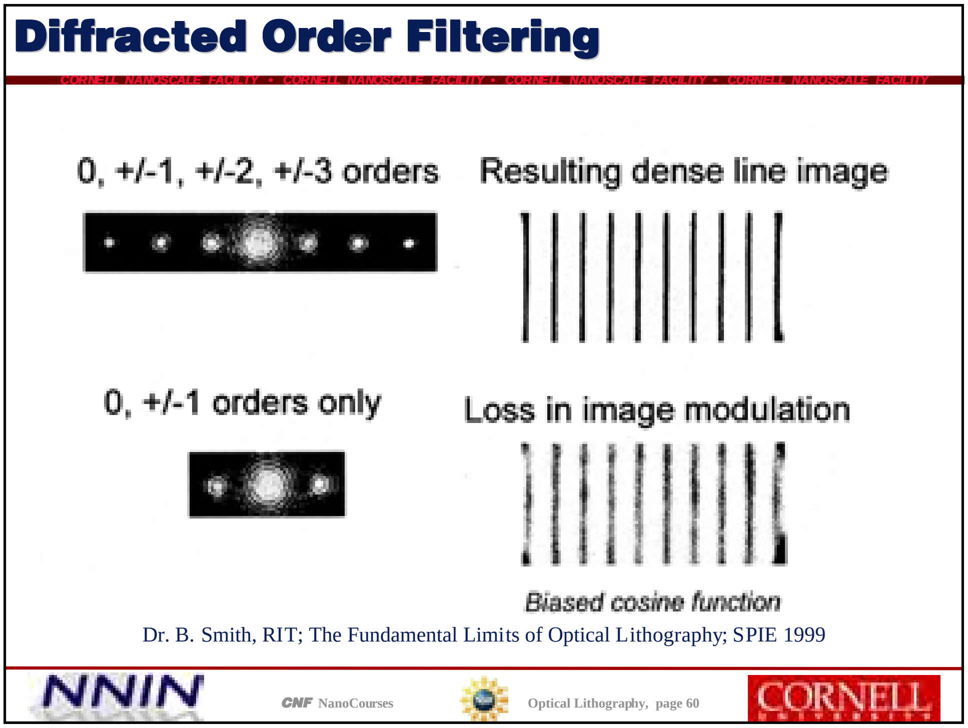




Lens Collection of Diffracted Orders

Minimum condition for imaging - more than 0th order

Dr. B. Smith, RIT; The Fundamental Limits of Optical Lithography; SPIE 1999



Diffracted Order Filtering

0, +/-1, +/-2, +/-3 orders

Resulting dense line image

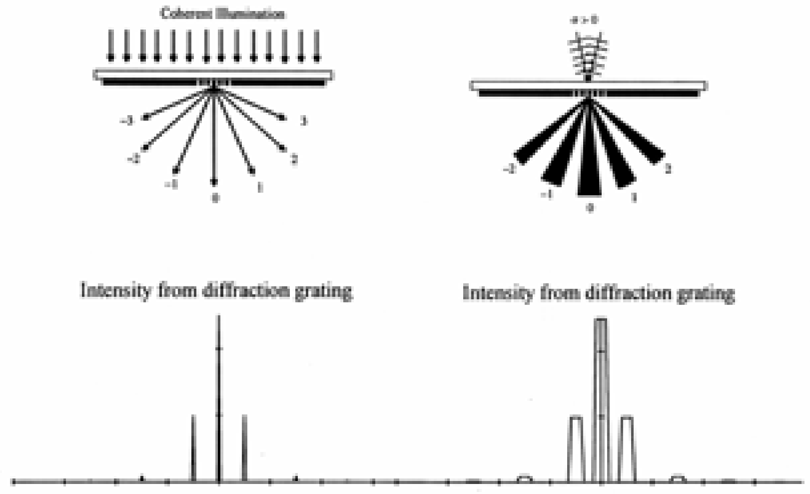
0, +/-1 orders only

Loss in image modulation

Biased cosine function

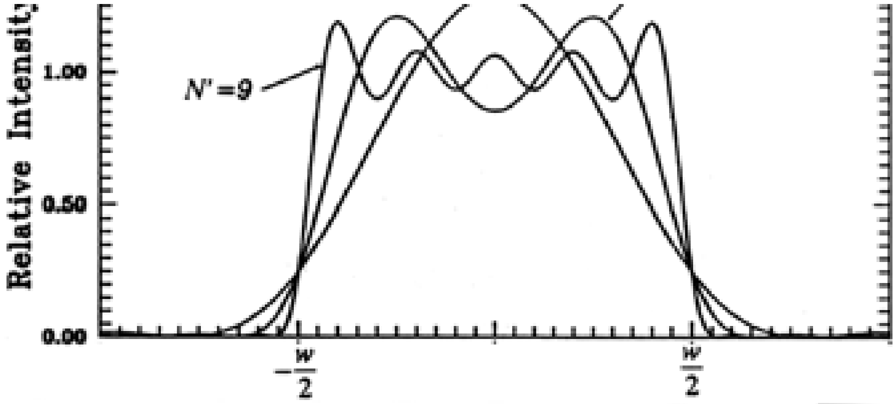
Dr. B. Smith, RIT; The Fundamental Limits of Optical Lithography; SPIE 1999

Partial Coherence vs. Resolution



Dr. B. Smith, RIT; The Fundamental Limits of Optical Lithography; SPIE 1999

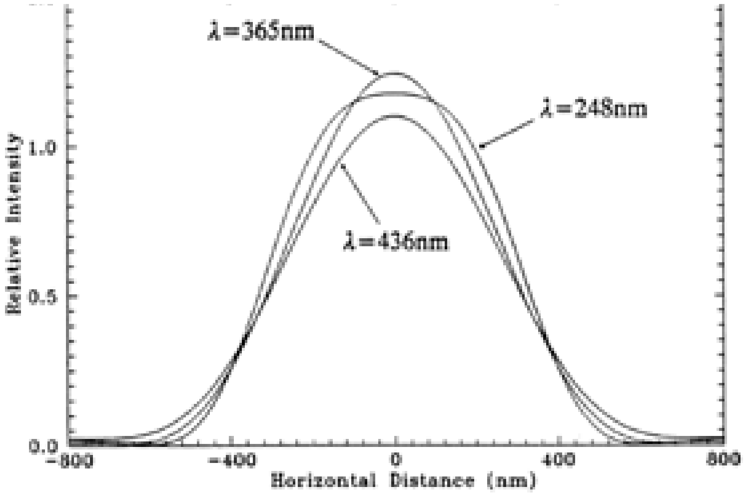
Aerial Image vs. Diffracted Order

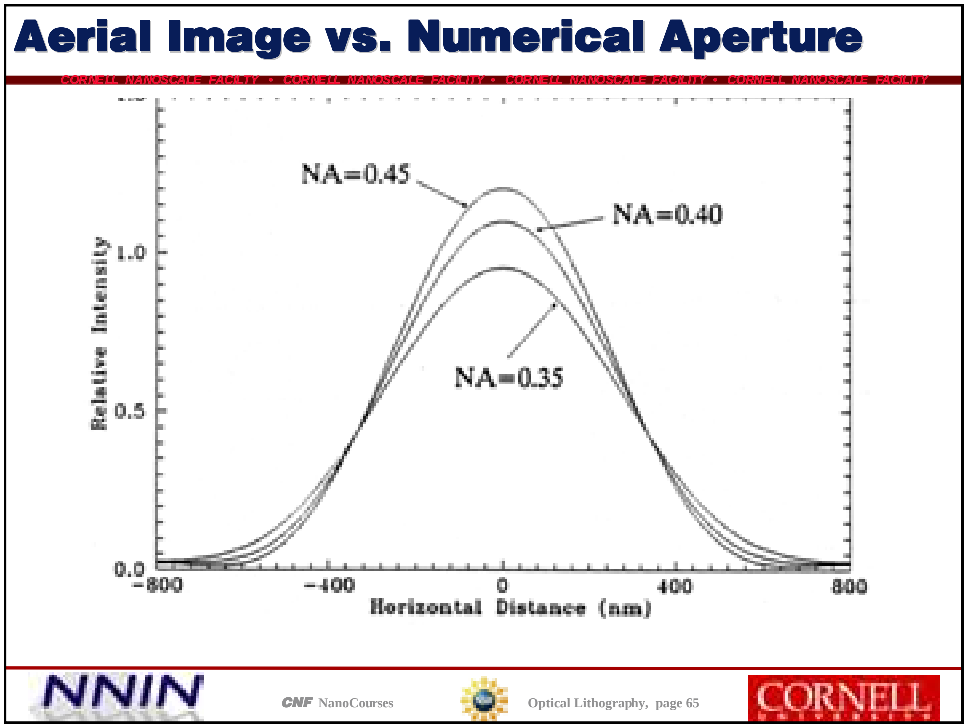


Optical Lithography Limits

- Minimum Feature Size
  - $d_{min} = k\lambda / \mathrm{NA}$
- Depth of Focus
  - $D = k\lambda / 2\,(\mathrm{NA})^2$

Aerial Image vs. Wavelength

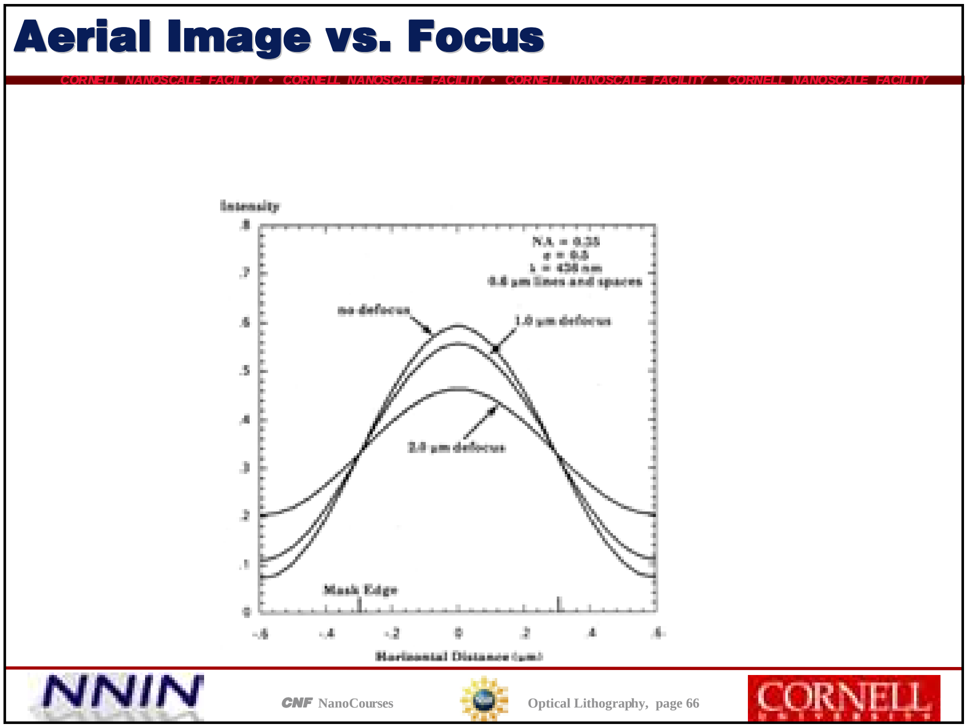




Aerial Image vs. Numerical Aperture

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

NNIN CNF NanoCourses Optical Lithography, page 65 CORNELL UNIVERSITY



Aerial Image vs. Focus

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

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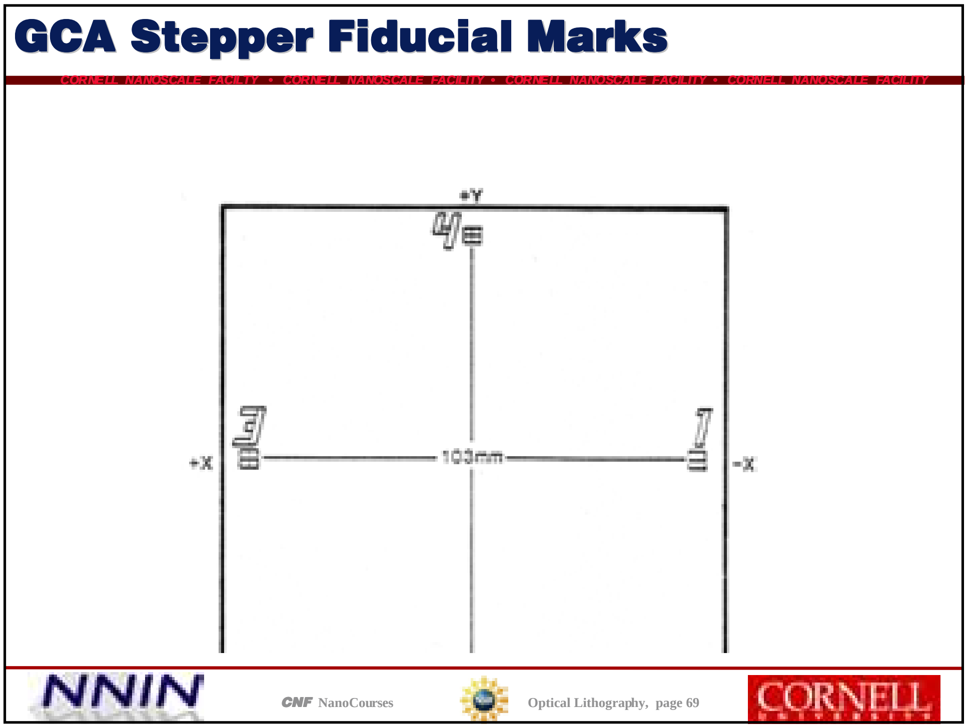
GCA Wafer Steppers

GCA 6300 5X or 10X

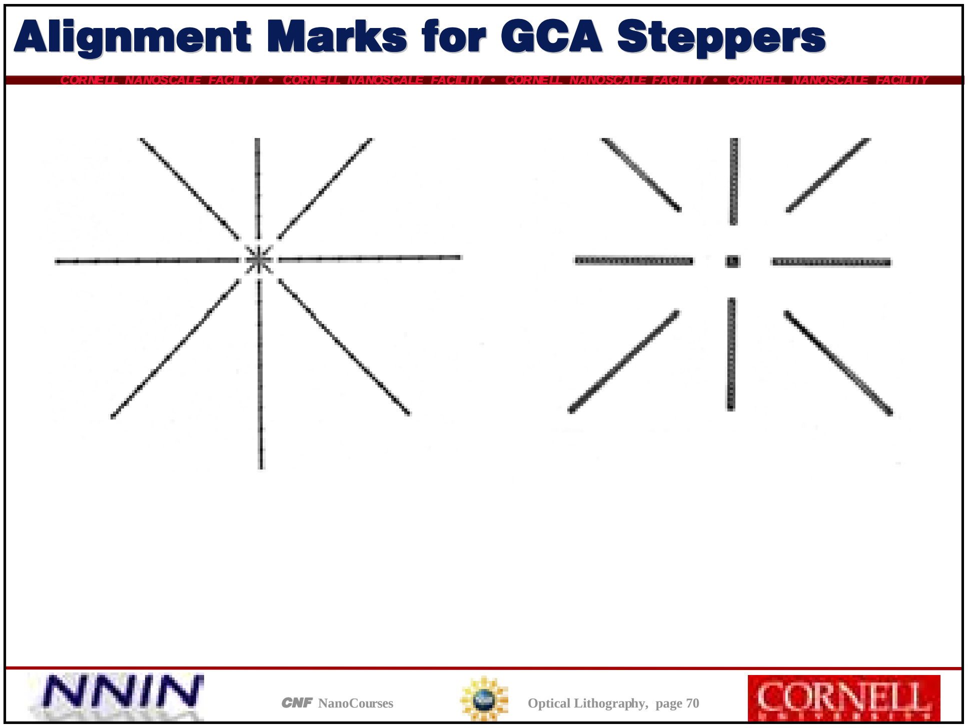
GCA Autostep 200

CNF Stepper Characteristics

cus			

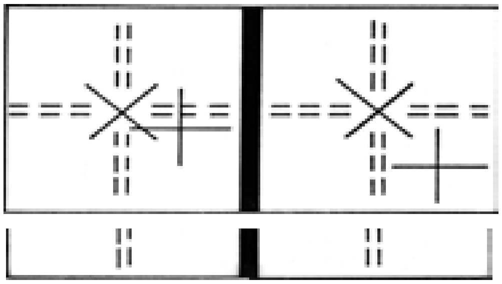


GCA Stepper Fiducial Marks



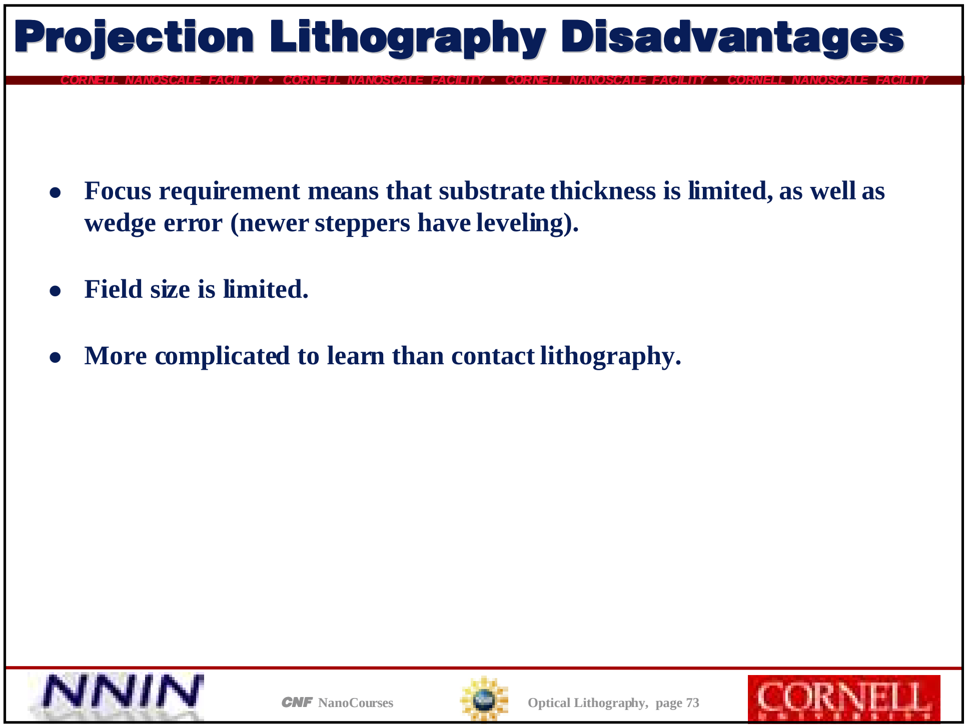
Alignment Marks for GCA Steppers

GCA Wafer Alignment



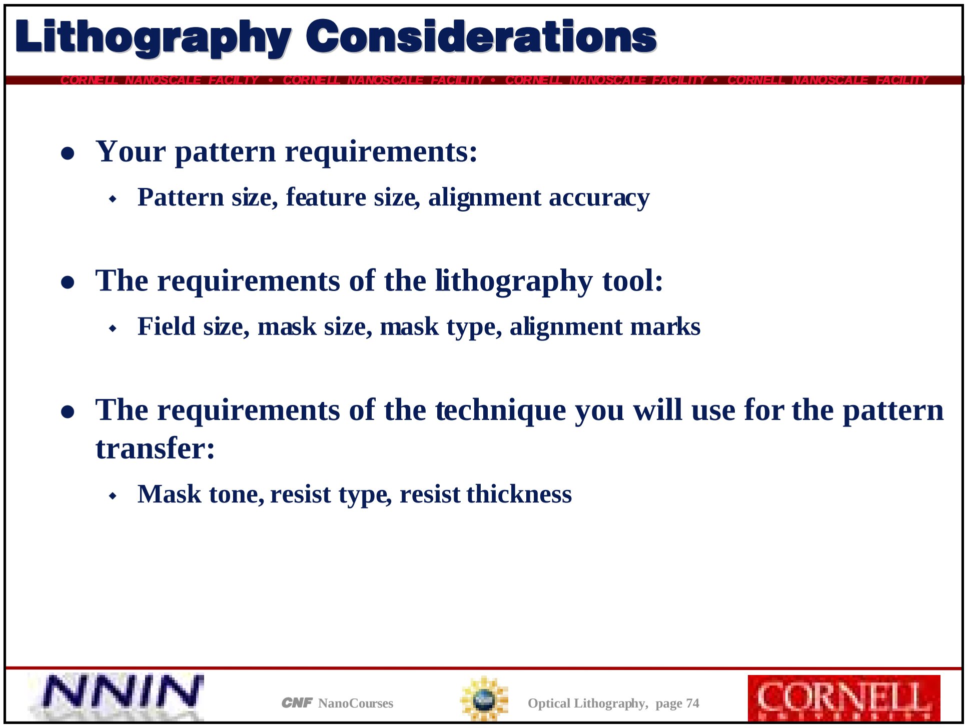
Projection Lithography Advantages

- Resolution comparable to the best contact lithography with no degradation of mask or resist.
- More tolerant of mask errors since mask image is reduced in size on the substrate. Almost all masks can be made on the PG.
- Step and repeat means many exposures per wafer, with the flexibility of computer control.
- Better alignment accuracy, typically ± 0.25 µm for the older GCA steppers.



Projection Lithography Disadvantages

- Focus requirement means that substrate thickness is limited, as well as wedge error (newer steppers have leveling).
- Field size is limited.
- More complicated to learn than contact lithography.



Lithography Considerations

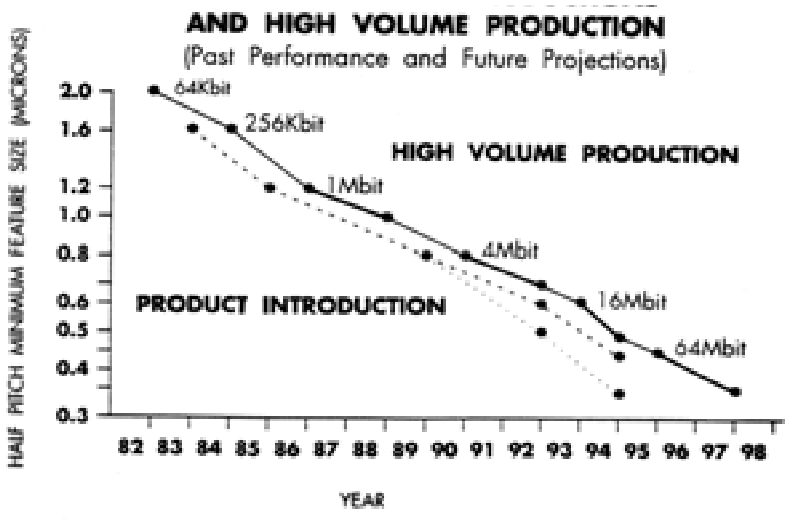
- Your pattern requirements:
  - Pattern size, feature size, alignment accuracy
- The requirements of the lithography tool:
  - Field size, mask size, mask type, alignment marks
- The requirements of the technique you will use for the pattern transfer:
  - Mask tone, resist type, resist thickness

Microlithography

Optical Lithography:

Techniques

Industrial Progress



Moore’s Law Continues

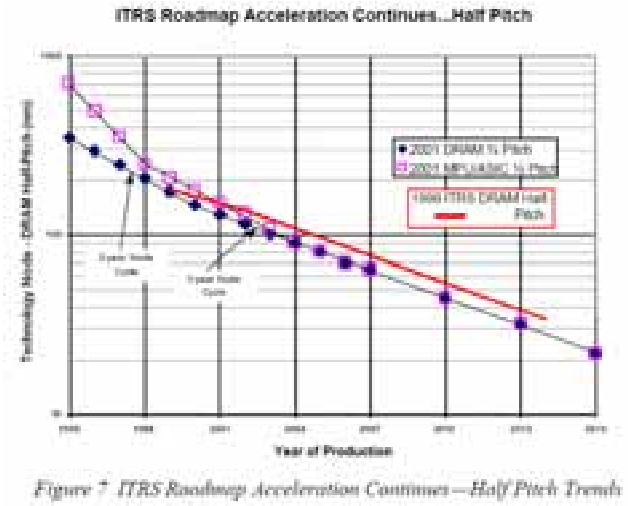


Figure 7 ITRS Roadmap Acceleration Continues—Half Pitch Trends

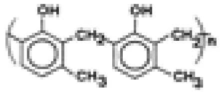
SIA Roadmap

Pentium 4 Die

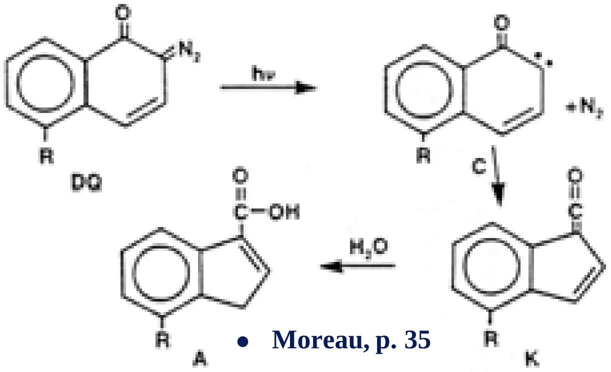
Intel Corp.

Photoresist Components

- Novolak Resin
- DNQ Photosensitizer

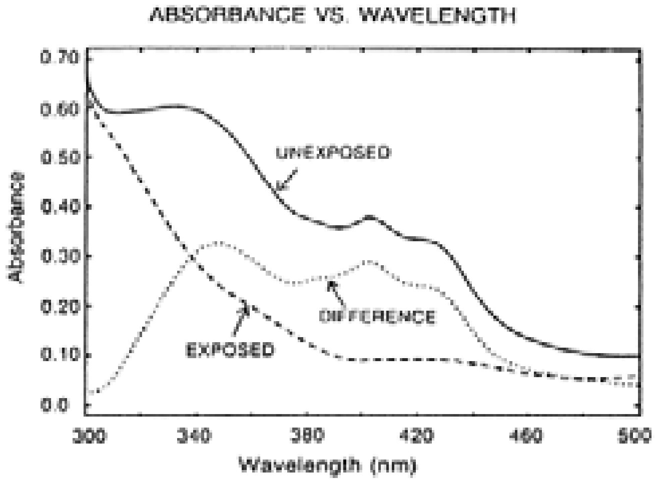


DNQ - Indene Carboxylic Acid



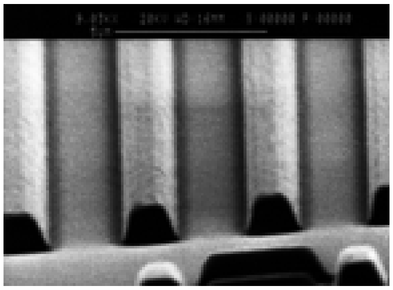
- Moreau, p. 35

Resist Absorbence Curve



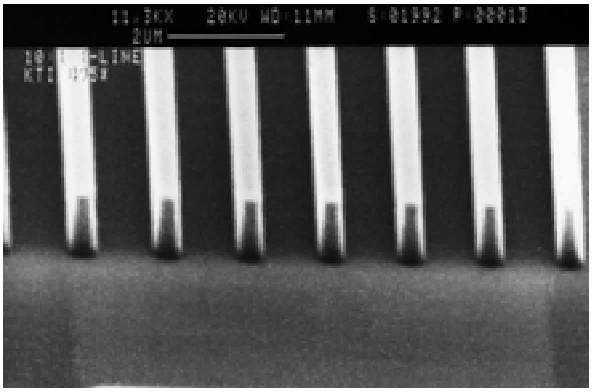
Shipley Product Information

Poor Resist Profile



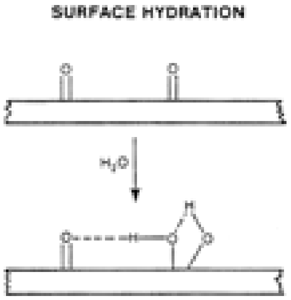
2.0 µm lines and spaces in 1.0 µm Shipley 1400 resist,
exposed with the 10:1 i-line stepper

Correct Resist Profile

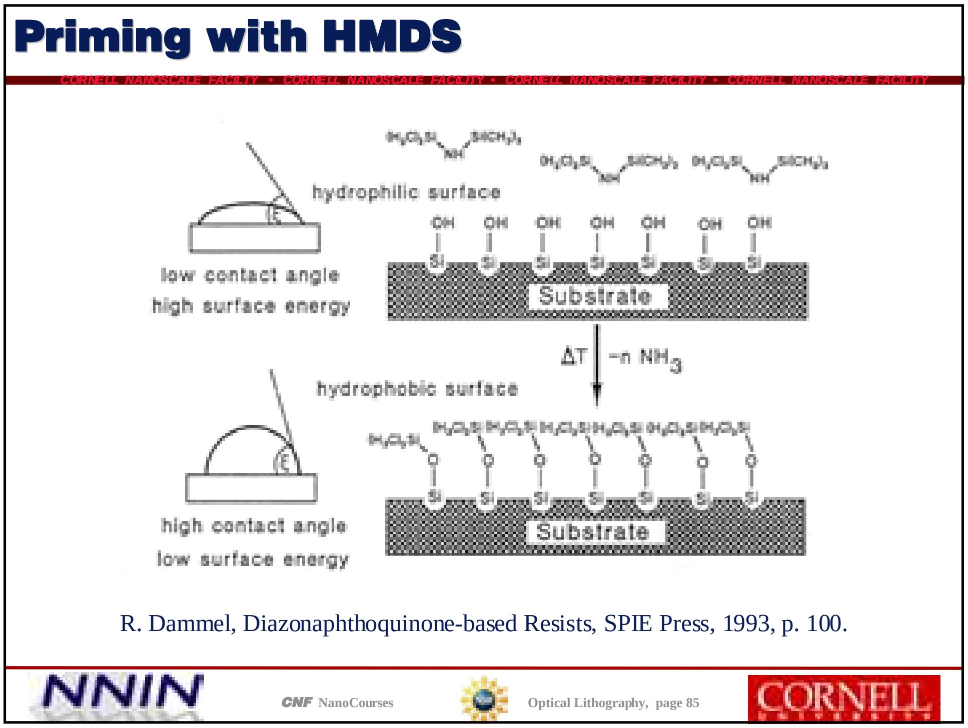


0.7 µm lines and spaces in 1.0 µm thick OCG 895i resist,
exposed with the 10:1 i-line stepper

Silicon Surface Hydration



Shipley Tutorial Graphics

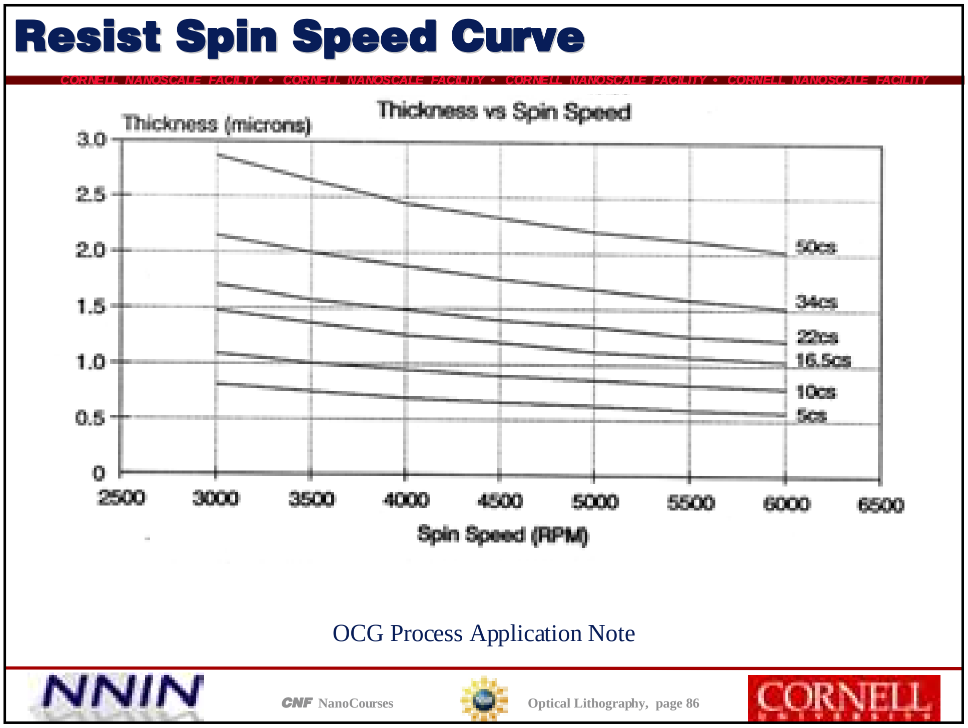


Priming with HMDS

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

R. Dammel, Diazonaphthoquinone-based Resists, SPIE Press, 1993, p. 100.

NNIN CNF NanoCourses Optical Lithography, page 85 CORNELL UNIVERSITY



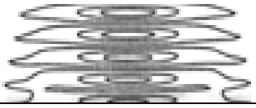
Resist Spin Speed Curve

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

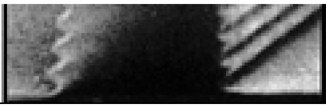
OCG Process Application Note

NNIN CNF NanoCourses Optical Lithography, page 86 CORNELL UNIVERSITY

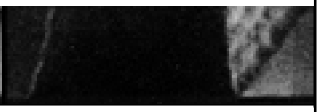
Standing Wave Effects



Calculated



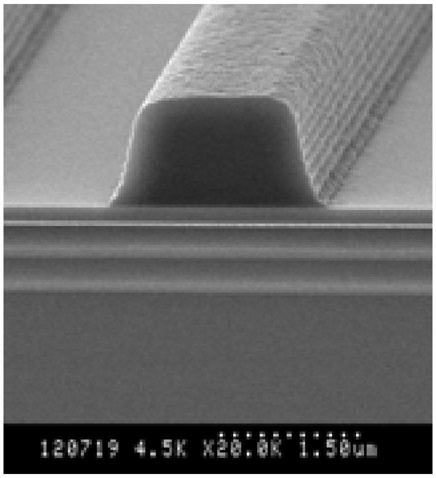
No PEB

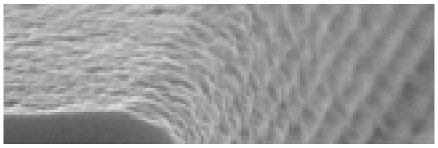


PEB, 115°C, 45 sec.

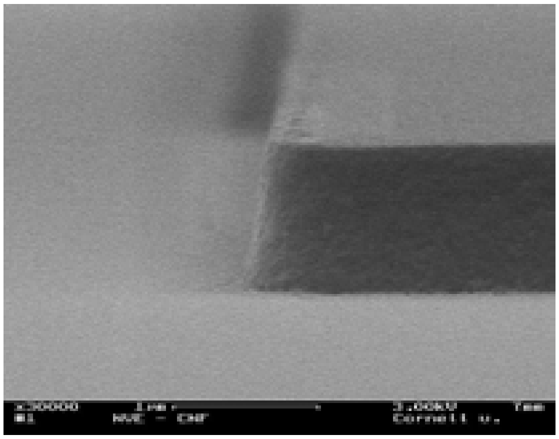
Dammel, p. 110.

Standing Waves





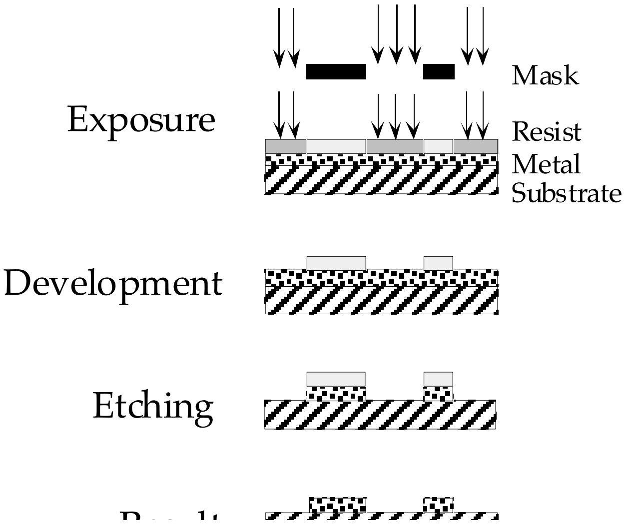
Resist Profile After Postbake



Resist Processing

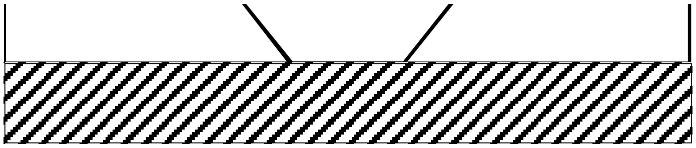
- Development
  - PEB
  - 300MIF, MF-321, MDC
  - Hardbake
- Stripping
  - Hot Strip Bath
  - 1165 Remover
  - O2 Plasma

Positive Tone Process



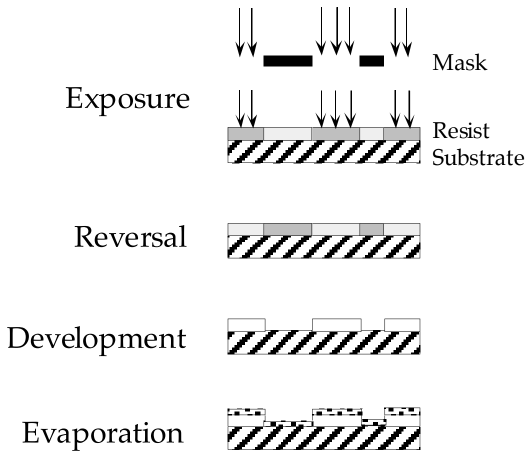
Positive Tone Sidewall Slope

- **After Development**



- **After Metalization**

Lift-off Using Image Reversal



Lift-off Process

- After Image Reversal

- After Metalization

Image Reversal

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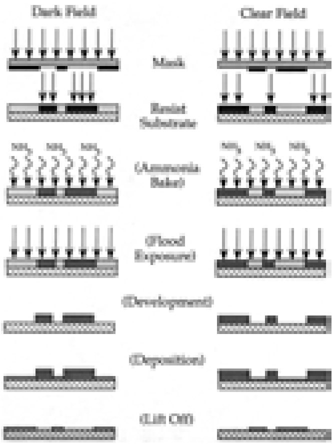
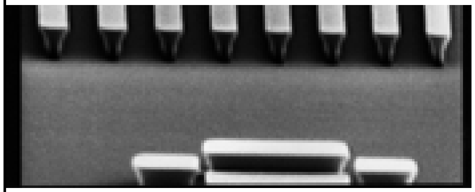


Image Reversed Resist Profile

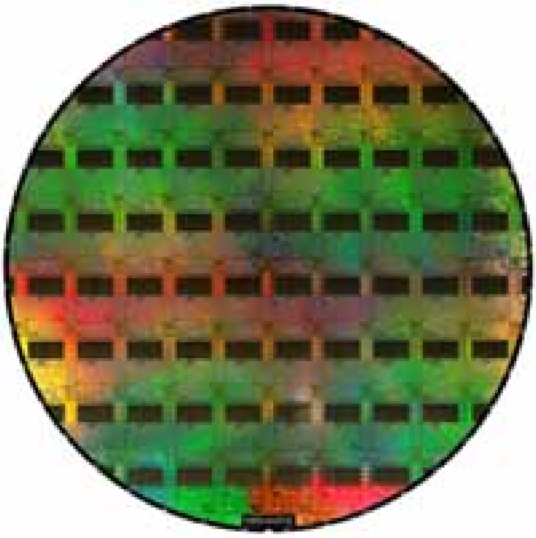
CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY



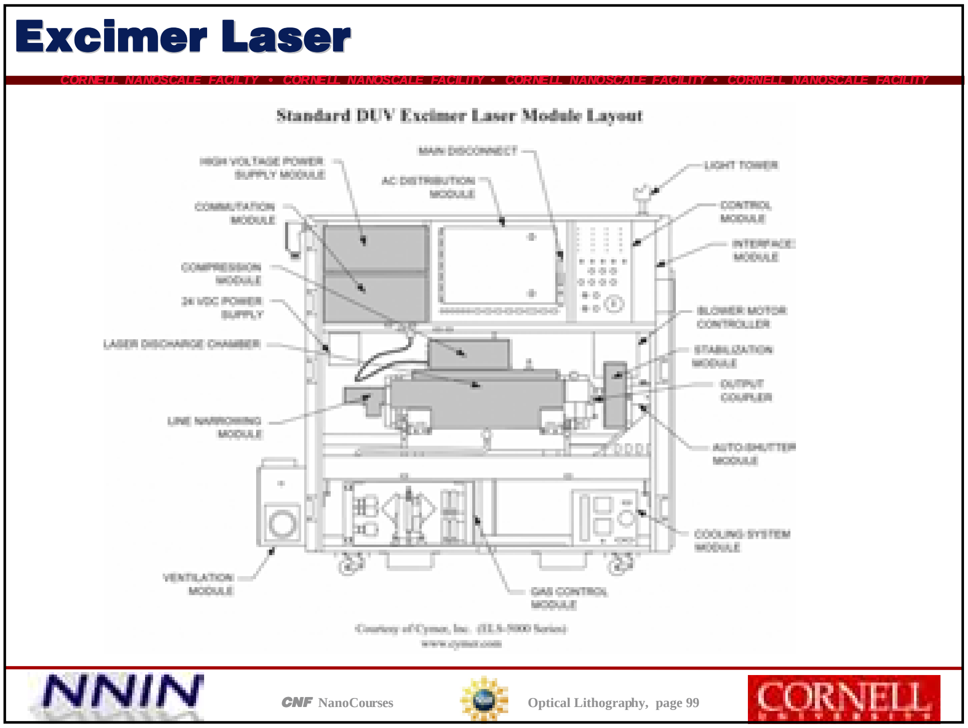
Summary of Considerations

- Your pattern requirements:
  - Pattern size, feature size, alignment accuracy
- The requirements of the lithography tool:
  - Field size, mask size, mask type, alignment marks
- The requirements of the technique you will use for the pattern transfer:
  - Mask tone, resist type, resist thickness

8” Intel Wafer



Intel Corp.



Excimer Laser

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Standard DUV Excimer Laser Module Layout

Courtesy of Cymer, Inc. (ELS-5000 Series)
www.cymer.com

NanoCourses 2004, Section 1

Practical Lithography:

The Art and Science of Microlithography

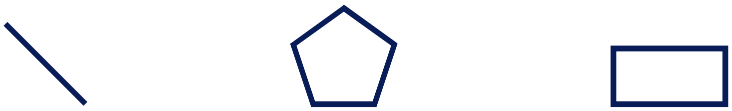
Computer-Aided Design (CAD)
by
Karlis Musa

Presented by the
***CNF* Technical Staff**
for the education of CNF Users,
Potential Users, and Industrial Sponsors

Pattern Layout and Translation …

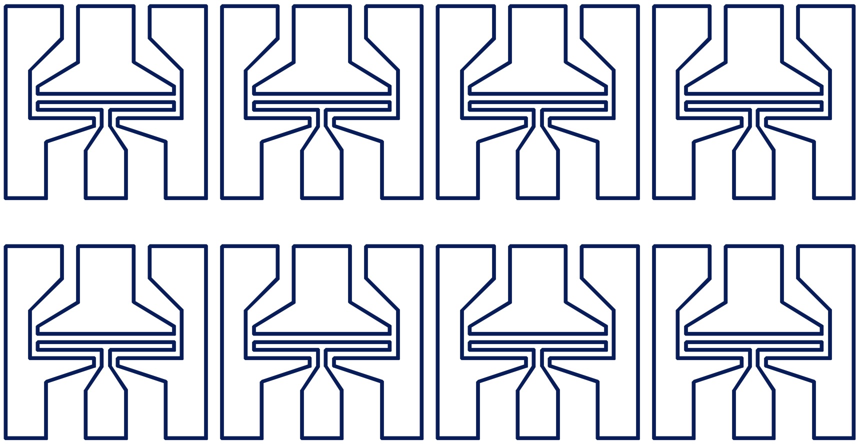
This part of the process is where you take what you think you want, and put it into a form that the instruments at the CNF will understand.

Typically, this starts with CAD, which uses lines, equations, polygons, algorithms, rectangles, etc…

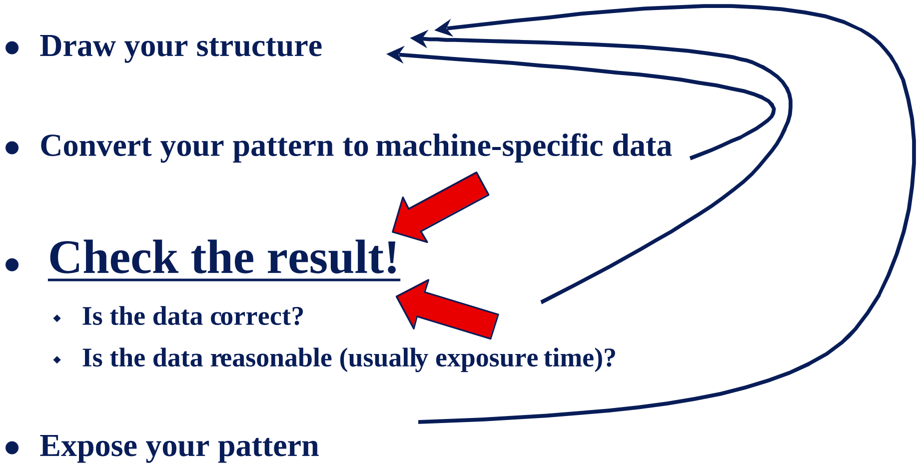


… Pattern Layout and Translation

… to create your pattern:



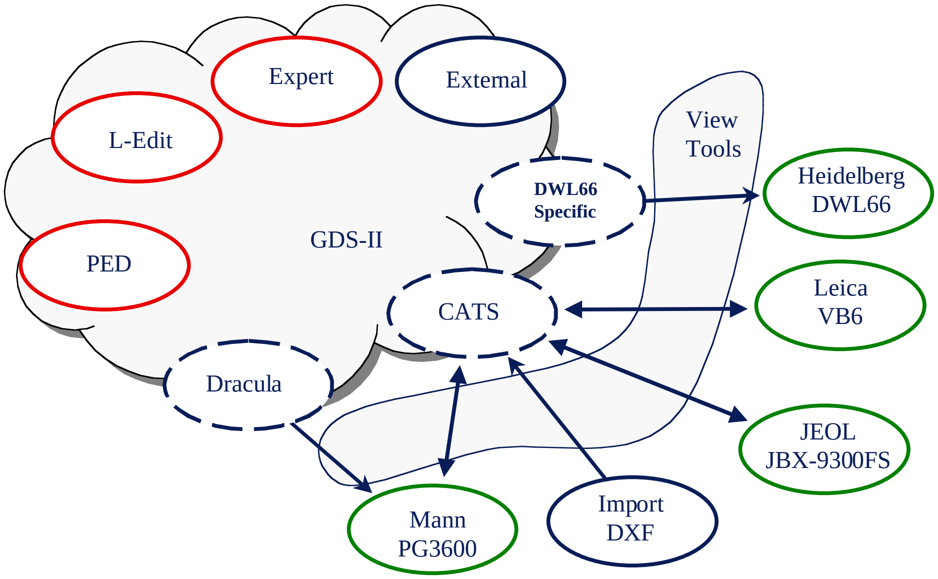
The Process



- Draw your structure
- Convert your pattern to machine-specific data
- Check the result!
  - Is the data correct?
  - Is the data reasonable (usually exposure time)?
- Expose your pattern

This is an evolutionary process!

The Overview



Some Terms

- **GDS** – industry standard format for the exchange of layout data. (aka GDS-II, aka STREAM).
- **User Units** – what the user sees as the units used for their patterns. Usually in microns. (Not the lower limit of what you can use.)
- **Internal Units** – how **User Units** are defined internally**.** Usually expressed as 1000 Internal Units per User Unit (1 nanometer).
- **Datatype –** mechanism for a user to optionally associate data with a particular object. At the CNF, most commonly used to provide exposure hints for e-beam patterns.
- **CIF** – another exchange format.
- **DXF** – AutoCAD text exchange format. We can read DXF. AutoCAD can be used for nanofabrication patterns, but there are better solutions.

Some More Terms

- **Alignment Marks –** Special sets of shapes that are used to align subsequent processing steps.
  - First part would be included during an exposure.
  - The second part would be included in the next exposure, to match up with the mark already on the wafer.
  - For additional exposures, you may need additional marks.
- **Fracture –** related to the process where your shapes are broken into much smaller shapes that the tool can expose.
  - **Mann PG** – Overlapping, rotated rectangles (2 µm to 1500 µm, in _ µm steps).
  - **E-Beam** – Quadrilaterals, and single-pass lines. Generally, overlaps are removed. Overlapping figures can be used to fine-tune an exposure.

Circles, and other curved figures …

… are supported by some CAD tools, BUT
• NOT by GDS, and
• NOT by the lithography tools.

Instead, they will be approximated by regular polygons, or a series of line segments. You control the accuracy of the approximation.

A more accurate approximation will usually take more time, more space, and more money.

The question to ask is:

“What is good enough?”

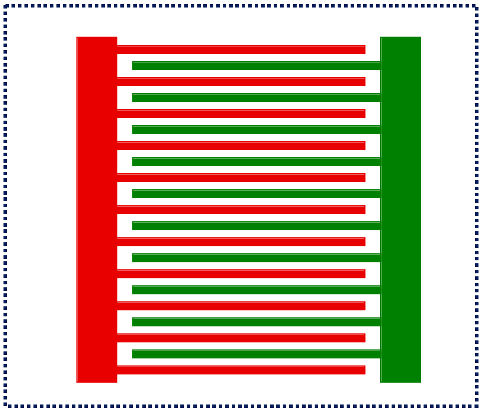
Layers

Lithography is a 2-D exposure that, after additional processing, results in a 3-D structure. **Layers** are the mechanism in CAD used to identify these exposure steps.

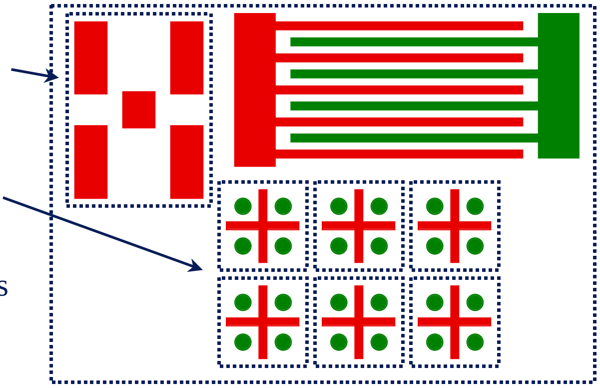
- Usually, a layer in CAD will translate to a single exposure (or mask).
- In some cases, it is useful to use multiple layers for a single exposure.
- There may be other layers, for additional information, layout guides, or tone-reversal.
- Layer definitions apply to all of the cells in a layout or library. However, a cell will typically not use all of these layers.

Cell

A **cell** is the basic building block of your pattern.



Cells



A cell can refer to other cell(s).

A cell can also refer to an array of another cell.

Any subsequent changes to the child cell will propagate.

Copy/Paste of the contents of one cell to another will **NOT** maintain this linkage, usually resulting in confusion and/or extra work.

Layout / Library

A **layout** (or **library**) is a collection of one or more cells, with one or more layers defined, plus some other information.

For very complex structures, one structure per layout.

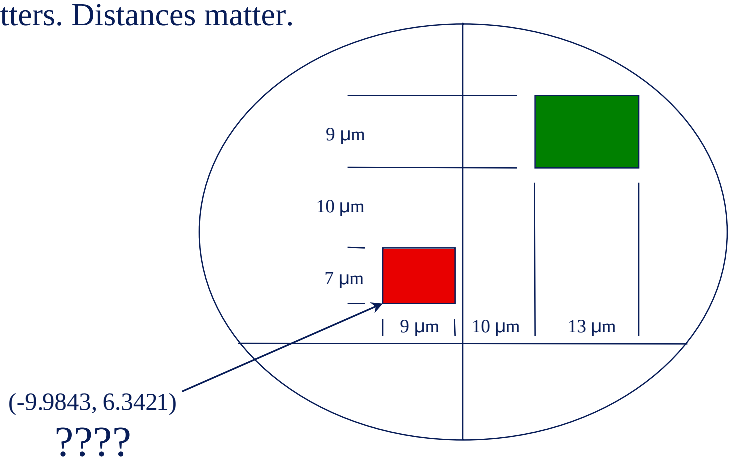
At the CNF, people will often have multiple structures in a single layout, but this is a personal choice, and not a technical one.

Where do I want to be?

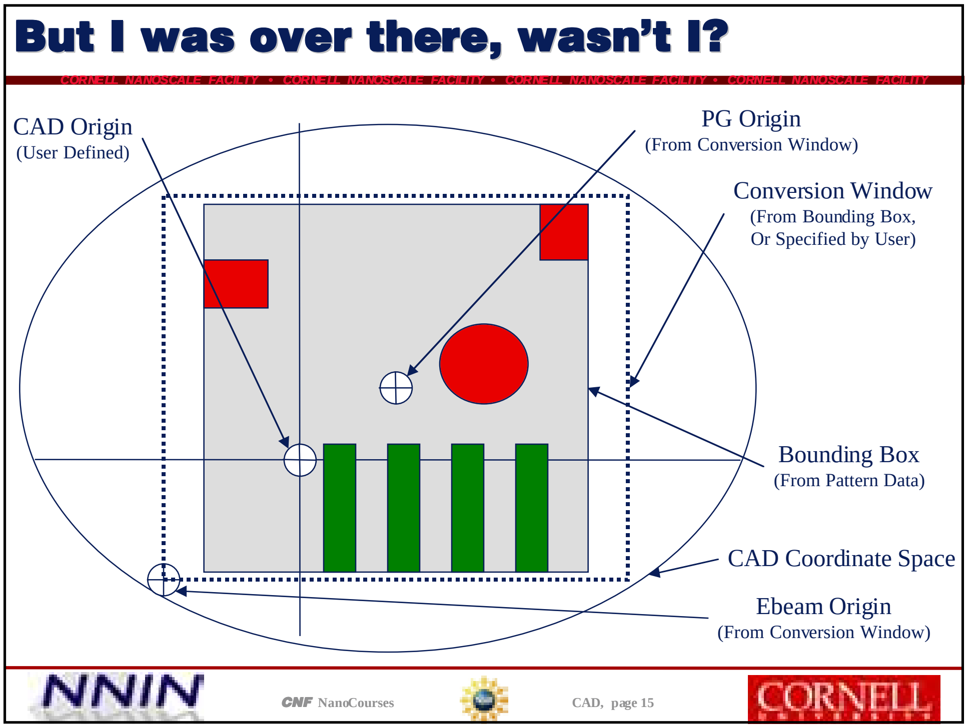
- Draw your structures actual size. The tool ultimately used to expose your pattern isn't significant at this time. This leaves your options open.
  - Any tool-specific scaling will be done during conversion.
  - The output of the conversion process is instrument-specific, the output of CAD is not.
  - Tone-reversal is usually done during conversion.
- **However,** some things **ARE** tool-specific…
  - Positional accuracy.
  - Alignment marks.
  - Performance characteristics.
  - …

I want to be where?

Size matters. Distances matter.



But, location also matters!



But I was over there, wasn't I?

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

CAD Origin
(User Defined)

PG Origin
(From Conversion Window)

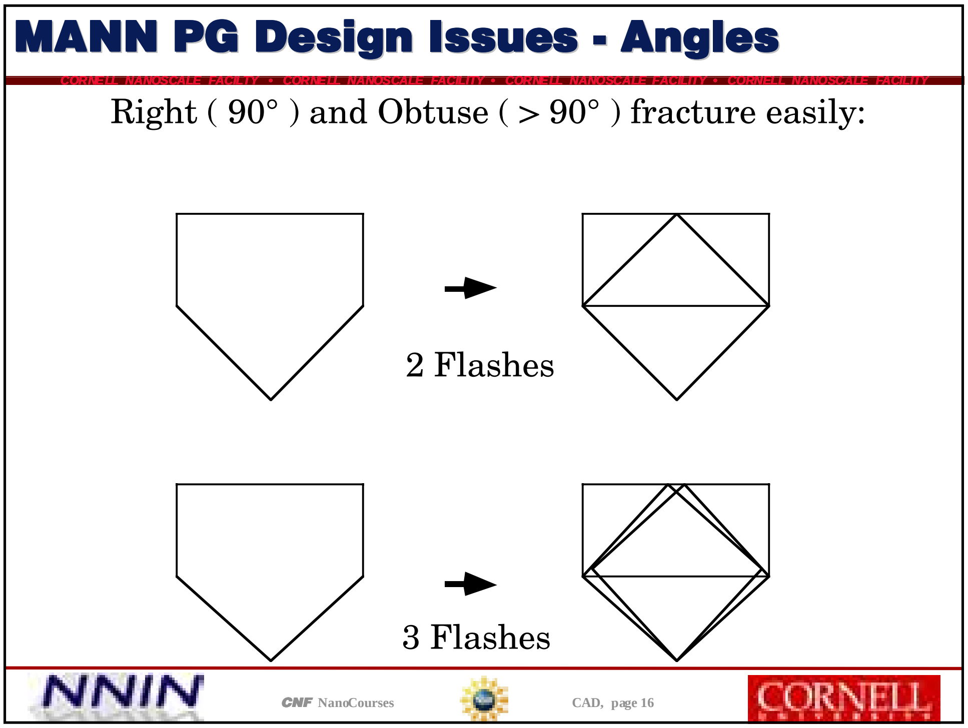
Conversion Window
(From Bounding Box,
Or Specified by User)

Bounding Box
(From Pattern Data)

CAD Coordinate Space

Ebeam Origin
(From Conversion Window)

NNIN CNF NanoCourses CAD, page 15 CORNELL UNIVERSITY



MANN PG Design Issues - Angles

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Right (90°) and Obtuse (> 90°) fracture easily:

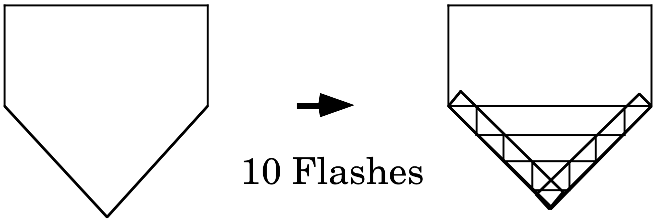
2 Flashes

3 Flashes

NNIN CNF NanoCourses CAD, page 16 CORNELL UNIVERSITY

MANN PG Design Issues - Angles

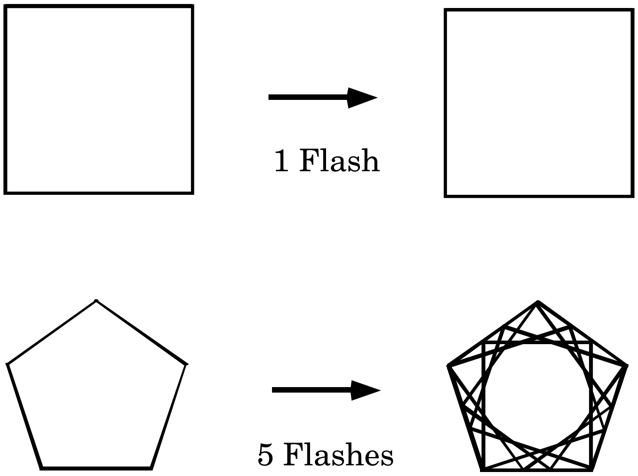
While Acute (< 90°) tend to suffer data explosion:



10 Flashes

MANN PG Design Issues - ‘Circles’

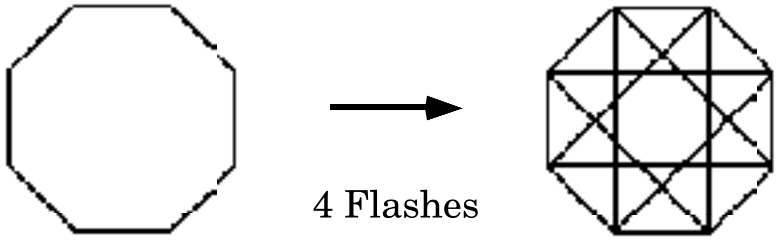
More sides on your circle mean more flashes on the PG



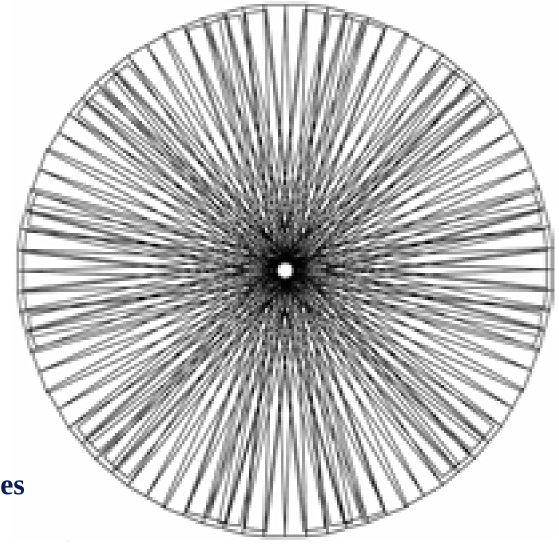
1 Flash

5 Flashes

MANN PG Design Issues - ‘Circles’



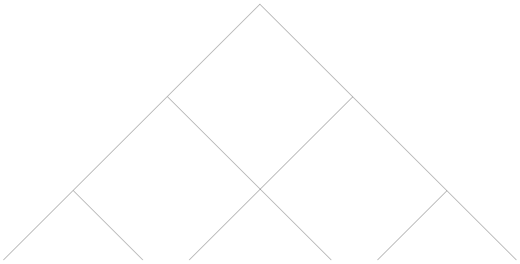
MANN PG Design Issues - ‘Circles’



80 sides result in 64 flashes
(r = 100 µm)

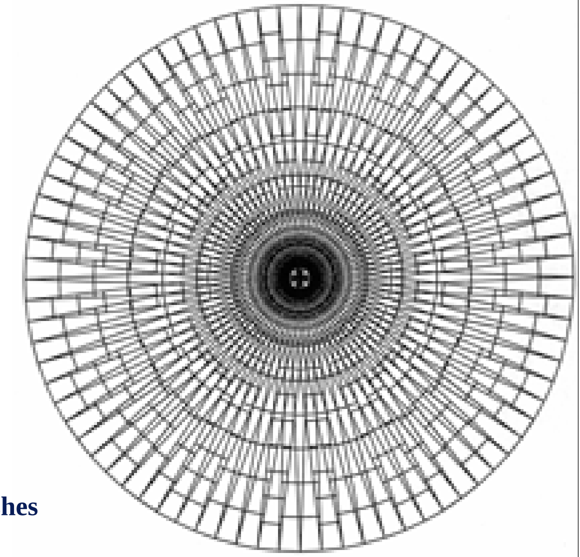
MANN PG Design Issues - ‘Circles’

It gets even worse once you exceed the aperture size

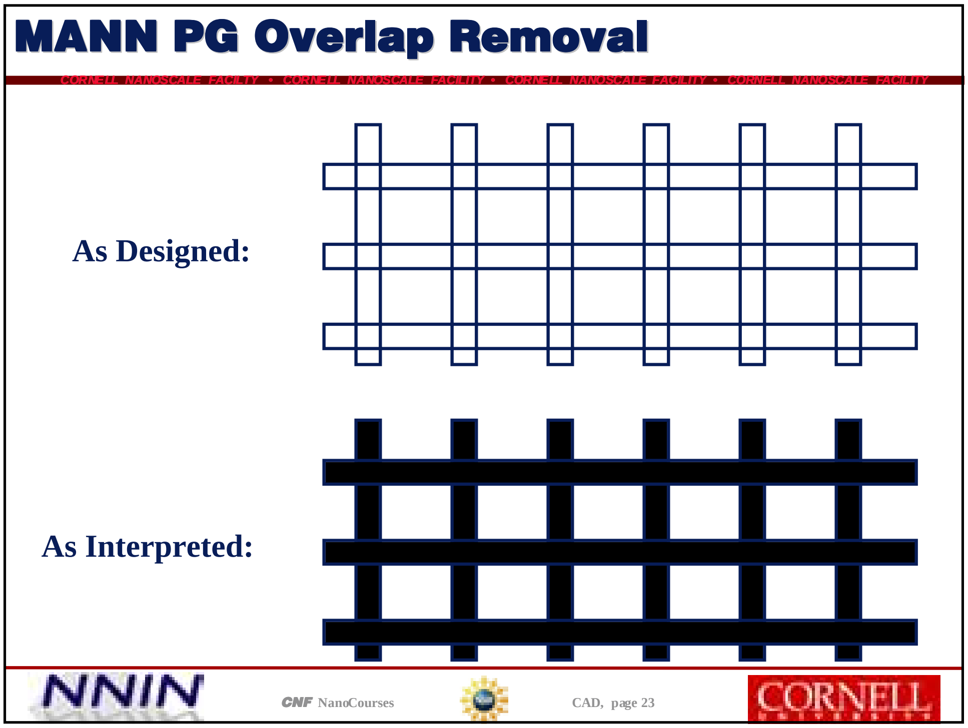


4 sides result in 9 flashes

MANN PG Design Issues - ‘Circles’



80 sides result in 1052 flashes
(r = 3000 µm)

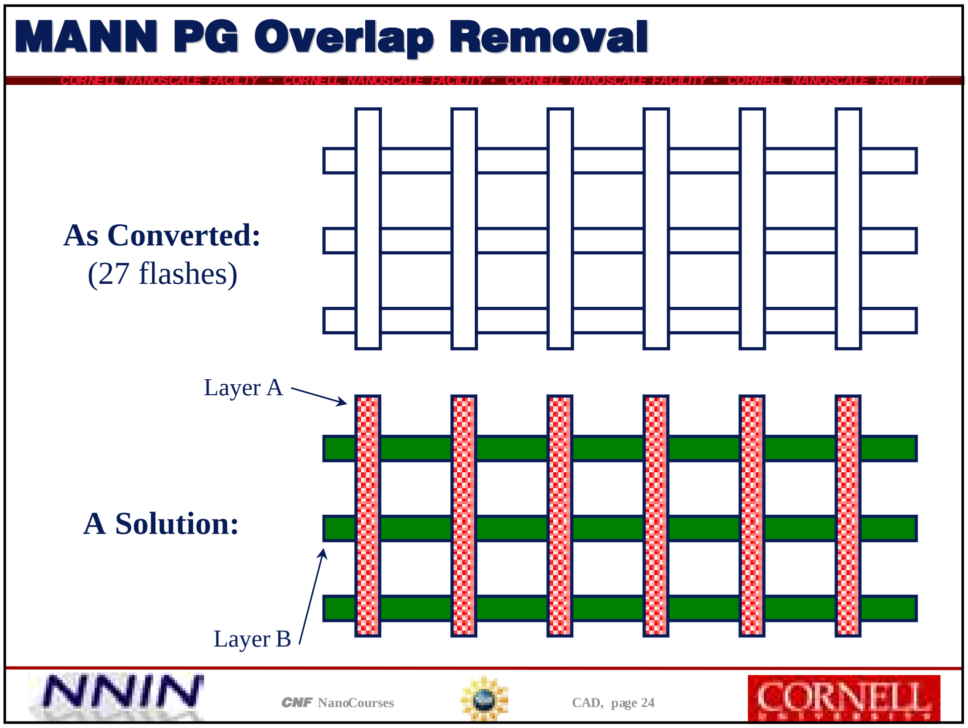


MANN PG Overlap Removal

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

As Designed:

As Interpreted:



MANN PG Overlap Removal

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

As Converted:
(27 flashes)

A Solution:

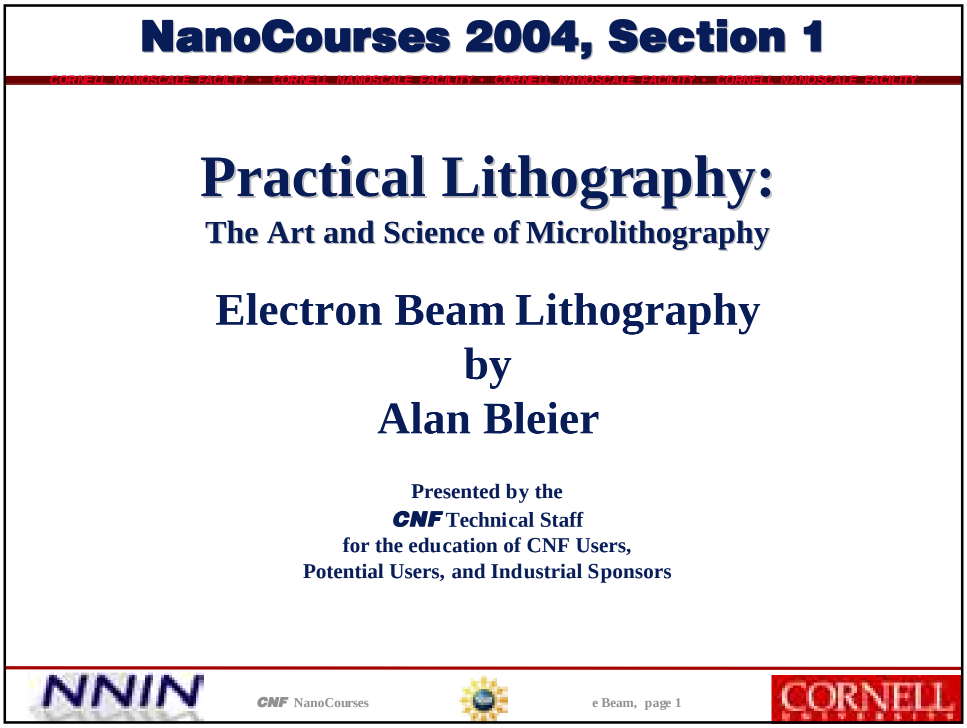
E-Beam Design Issues

- The maximum area that the electron beam can trace at one time is called an exposure FIELD.
- A pattern larger than this field will require stage motion.
- The intersections between fields are called STITCHING LINES.
- STITCHING ERRORS occur along these lines.

- Therefore, keep small features in the center of the field!

GDS Issues

- GDS is a binary format – if you are using FTP (or similar) to transfer, make sure that it transfers as Binary (or Image).
- There are various flavors of the GDS specification. There are also ‘enhancements’ that various companies made.
  - Uppercase cell names are easier. (For instance, L-Edit has an export option that will do this for you.)
  - Some software will generate polygons with thousands of vertices. 200 or less works much better.



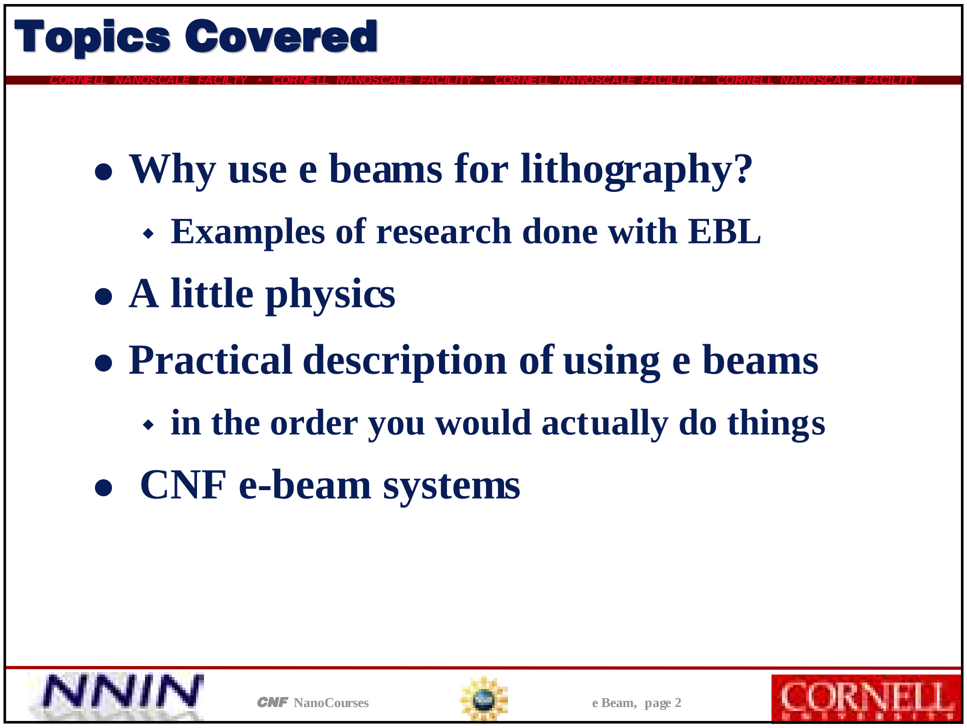
NanoCourses 2004, Section 1

Practical Lithography:

The Art and Science of Microlithography

Electron Beam Lithography
by
Alan Bleier

Presented by the
CNF Technical Staff
for the education of CNF Users,
Potential Users, and Industrial Sponsors



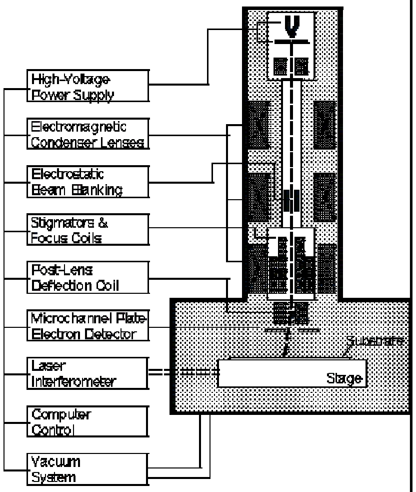
Topics Covered

- Why use e beams for lithography?
  - Examples of research done with EBL
- A little physics
- Practical description of using e beams
  - in the order you would actually do things
- CNF e-beam systems

What is Electron Beam Lithography?

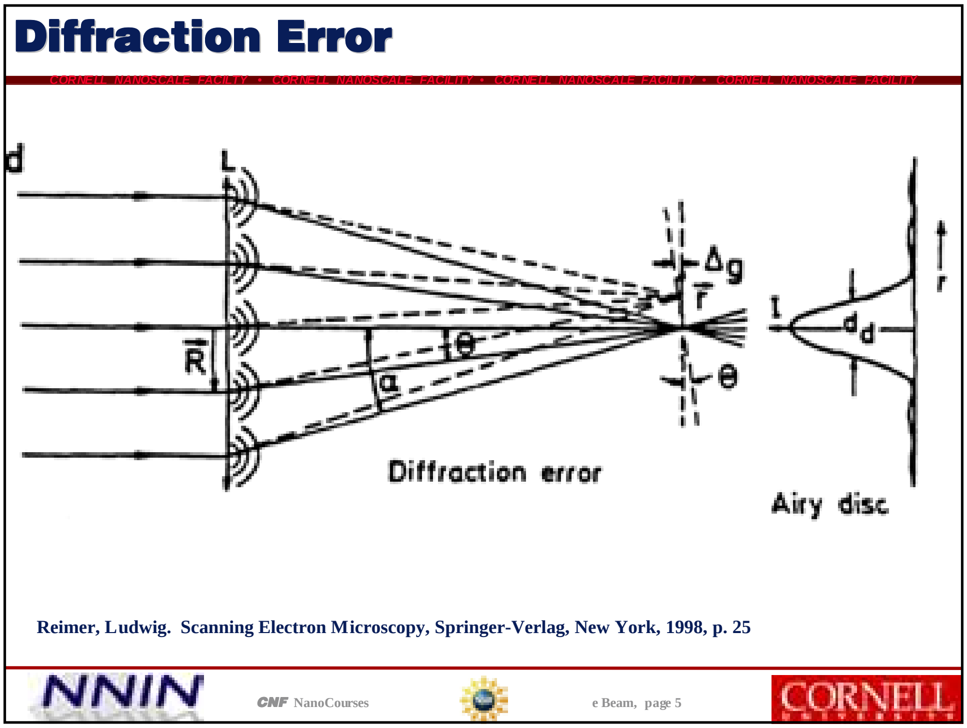
- Focused beam of electrons
- Computer driven pattern generator
- Serially expose individual points to create a pattern (direct write)
- Alternatively, expose rectangular or triangular patches (shaped beam) or project sections of a pattern (e.g. PREVAIL, SCALPEL)
- Irradiation causes chemical change in resist
- Latent image developed by selective solution

Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.2.html



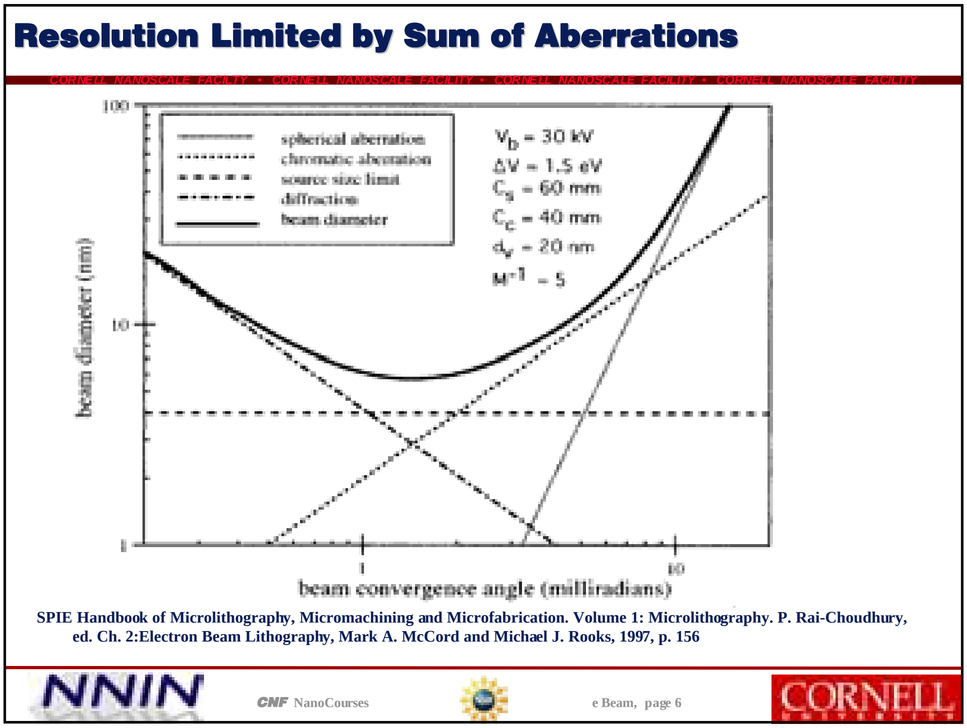
Why Use Electron Beams?

Optical Lithography	e-Beam Lithography
High speed for large shapes	High speed for complex Patterns
High Speed, Parallel Exposure	Point by Point Exposure Limits Speed
Light Diffraction Limits Minimum Feature Size to 50 nm at best	Not Diffraction-limited; Resolution 20 nm



Diffraction Error

Reimer, Ludwig. Scanning Electron Microscopy, Springer-Verlag, New York, 1998, p. 25



Resolution Limited by Sum of Aberrations

SPIE Handbook of Microlithography, Micromachining and Microfabrication. Volume 1: Microlithography. P. Rai-Choudhury, ed. Ch. 2:Electron Beam Lithography, Mark A. McCord and Michael J. Rooks, 1997, p. 156

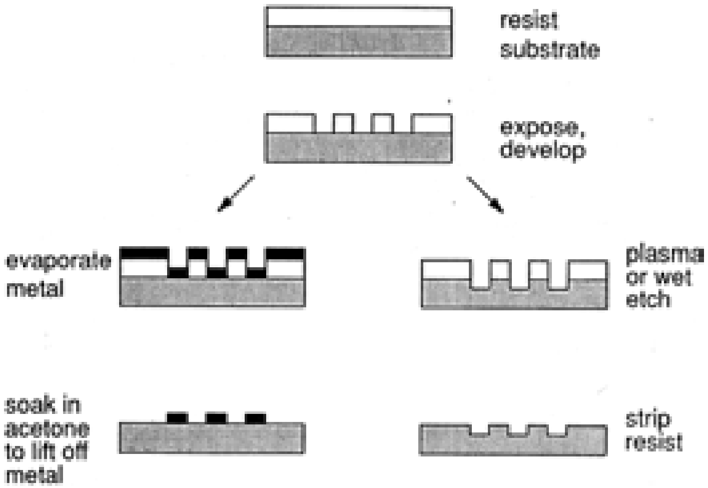
History of SEM and e-Beam Lithography

- 1926 H. Busch (Berlin) – Theory of electron trajectories
- 1939 Knoll & Theile (Berlin) – First SEM, 100 µm spot
- 1939 von Ardenne (Berlin) – First good SEM,0.1 µm spot
- 1948 C. W. Oatley & D. McMullan (Cambridge) – First modern SEM using two scan coils and secondary electron collector
- 1965 R. F. W. Pease & W. C. Nixon (Cambridge) – Everhart-Thornley detector used in prototype of first commercial SEM: Cambridge Mark I
- 1965 IBM, Cambridge, Hughes experiments with first beam writing using pump oil contamination and low-resolution Kodak resists
- 1971 M. Hatzakis, A. Broers, E. Wolf – PMMA for 60 nm lines
- 1974 EBES (Bell Labs) commercial e beam system, later spun off to Perkin Elmer
- 1985 National Nanofabrication Facility purchases JEOL JBX5DII

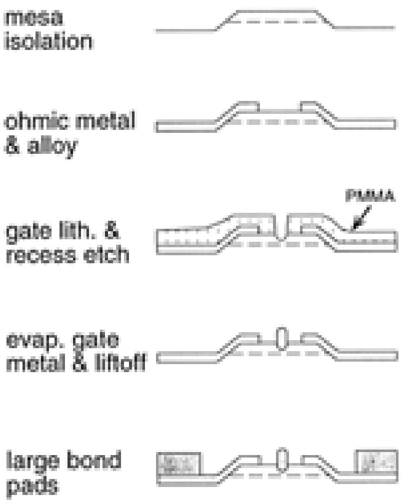
Examples

e-Beam Process Example

- Lithography and Pattern Transfer

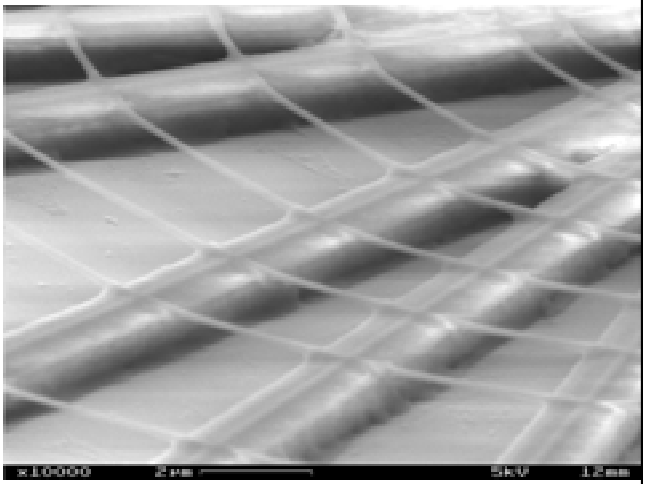


Example Mixed Optical & e-Beam: GaAs FET



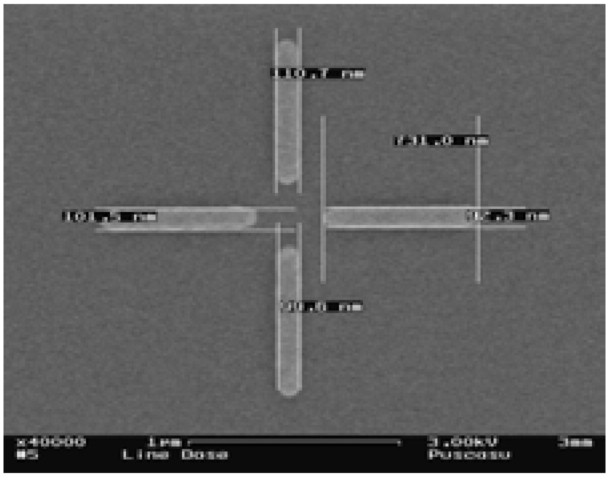
Research Done With Nabity NPGS on LEO SEM

- Dual Exposure Glass Layer Suspended Structures (DEGLaSS)
- David Tanenbaum (Pomona College)
- Anatoli Olkhovets and Lidija Sekaric (Cornell)
- Amorphous Glass, Hydrogen Silsesquioxane (HSQ).



- 1 - 3 keV for suspended layers
- 3 - 20 keV for support structures

Research Conducted With Leica EBMF

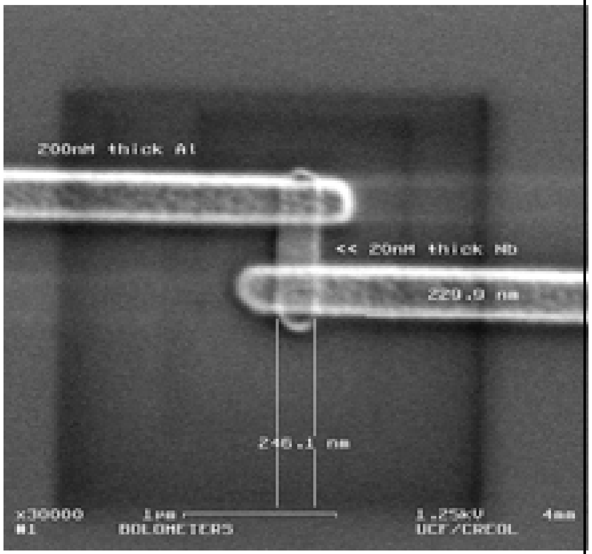


IR Crossed Dipole Resonant Filter

Glenn Boreman group (U. of Central Florida)

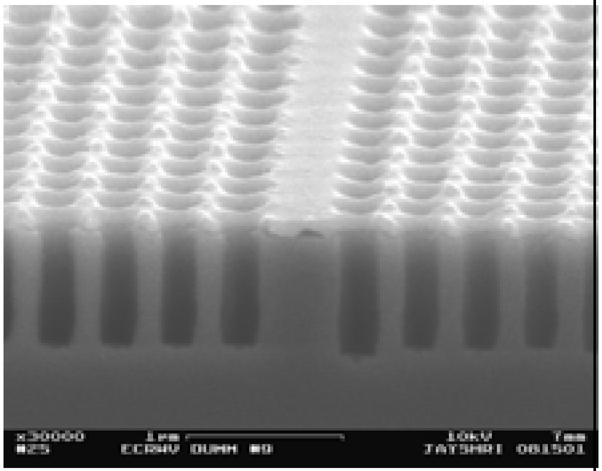
Infrared Antennas

- Glenn Boreman group (U. of Central Florida)
- ~ 200 nm Al leads
- Nb bolometer



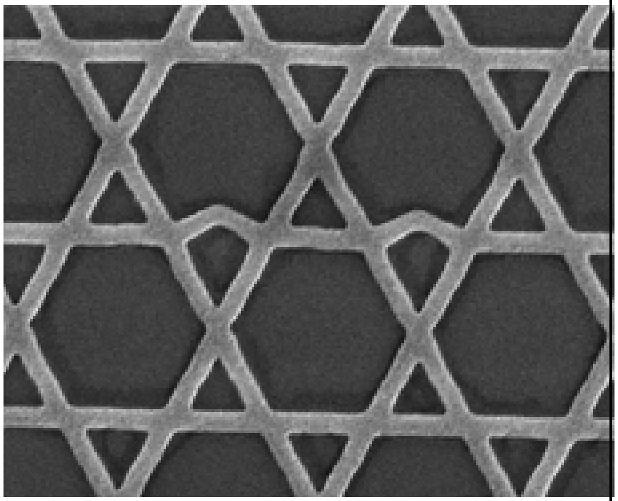
Photonic Crystal Microcavity InP-based Devices

- Jayshri Sabarinathan, Pallab Bhattacharya (U of Michigan)
- EBMF writes the reverse of the pattern on oxide (on top of InP/GaAs device). Then using dry etch and liftoff, reverse the pattern. Etched in the ECR tool
- Minimum feature sizes from 100 to 200 nm



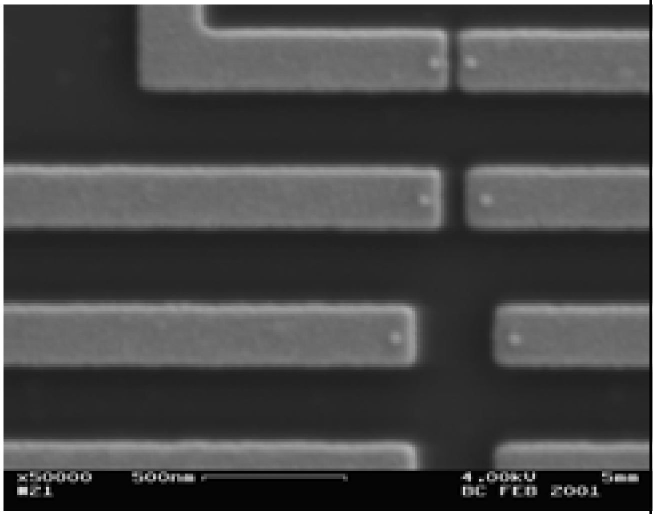
Disordered Superconducting Networks

- Yi Xiao (Princeton University)
- 1 mm Kagome structure with random defects
- 180 nm wide wires 50 nm Al liftoff array, 50 nm Au liftoff leads and contacts



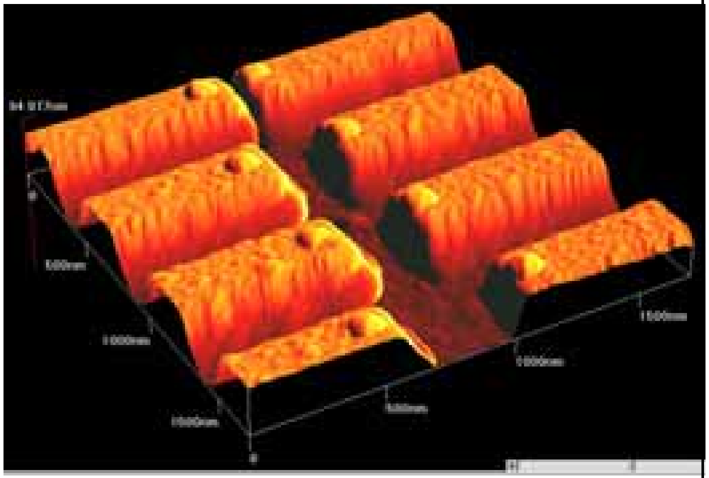
Addressable Carbon Nanotube Arrays

- Joel Moser, Michael Naughton (Boston College)
- Array of 40 nm Ni dots on platinum leads for carbon fiber growth and molecular attachment



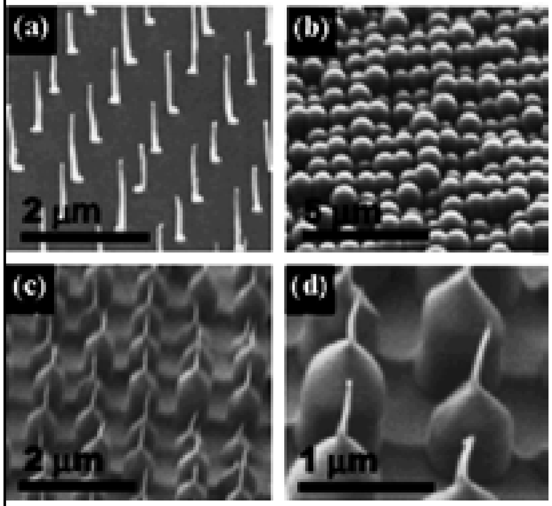
Addressable Carbon Nanotube Arrays

- ATM Image
- Patterned on Leica VB6
- Small dots made with aligned second exposure



- Joel Moser, Michael Naughton (Boston College)

Carbon Nanofibers for Field Emission Devices



- Michael Guillorn, Michael Simpson (U. Tennessee, Knoxville)
- Arrays of programmable e^- emitters made of vertically-aligned carbon nanofibers (VANCF)
- 50 nm dots on 50 nm pitch, drawn as 40 nm octagons
- Fibers grown by e gun PVD

Collective Magnetic Reversal Behavior of Interactive Particle Arrays

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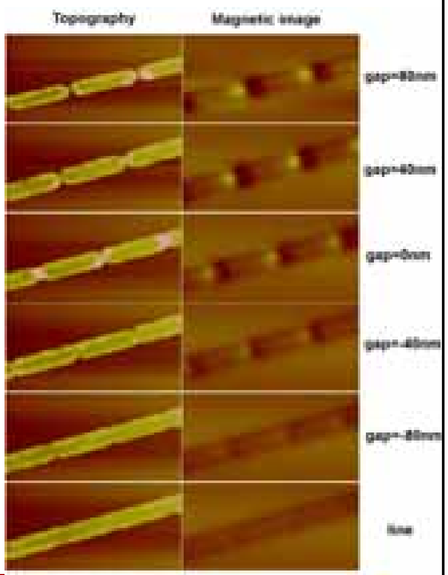
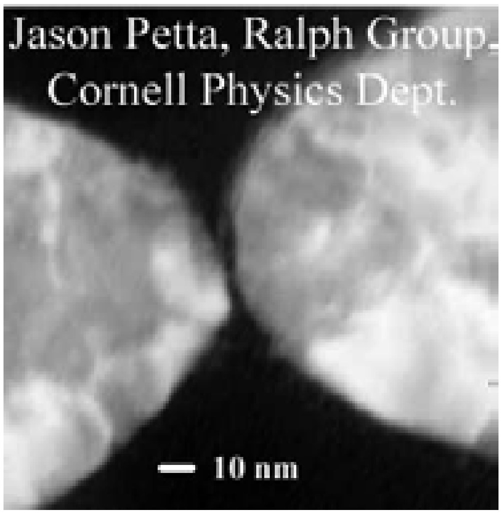
- Hyuncheol Koo, R. D. Gomez (U. of Maryland)
- Island size 300 nm by 900 nm
- Magnetic dipole at the ends of island - dark and bright
- The neighboring island produces stray field which may change the switching characteristics of islands



Physics of nm-Scale Superconductors and Magnets

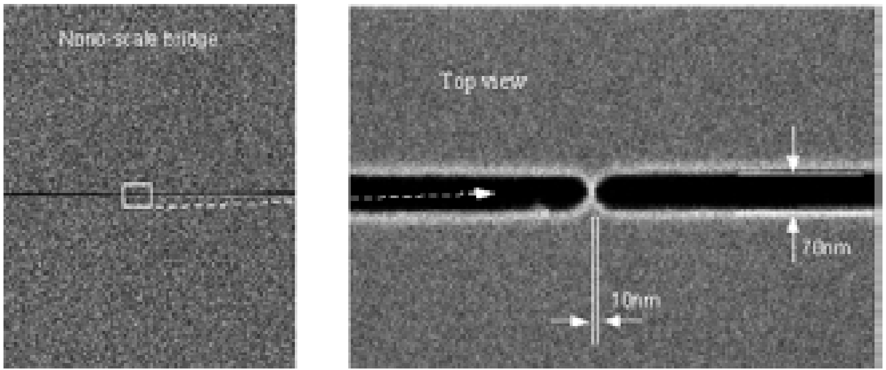
CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

- Two Au electrodes exposed in two separate steps
- Second electrode aligned to the first using the VB6
- By changing the offset between the electrodes, can typically obtain sub-10 nm gaps


Jason Petta, Ralph Group, Cornell Physics Dept.

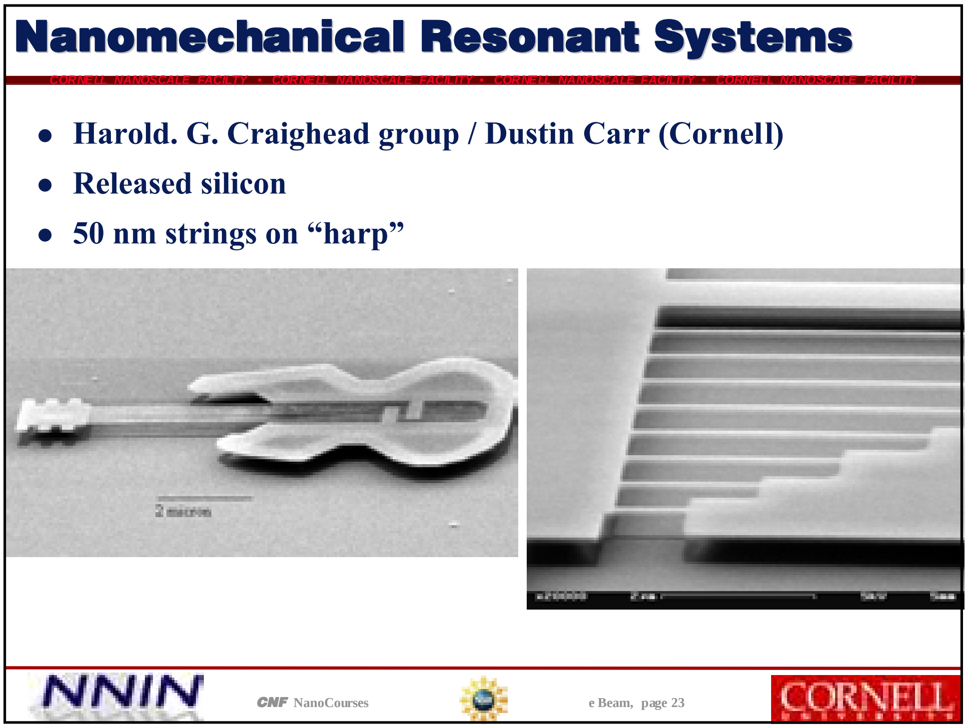
Physics of Atomic-Scale Conducting Objects

- Dragomir Davidovic (Georgia Inst. of Technology)
- Investigates electron transport in atomic-scale diameter contacts between metals and single molecules bridging atomic scale gaps between metals



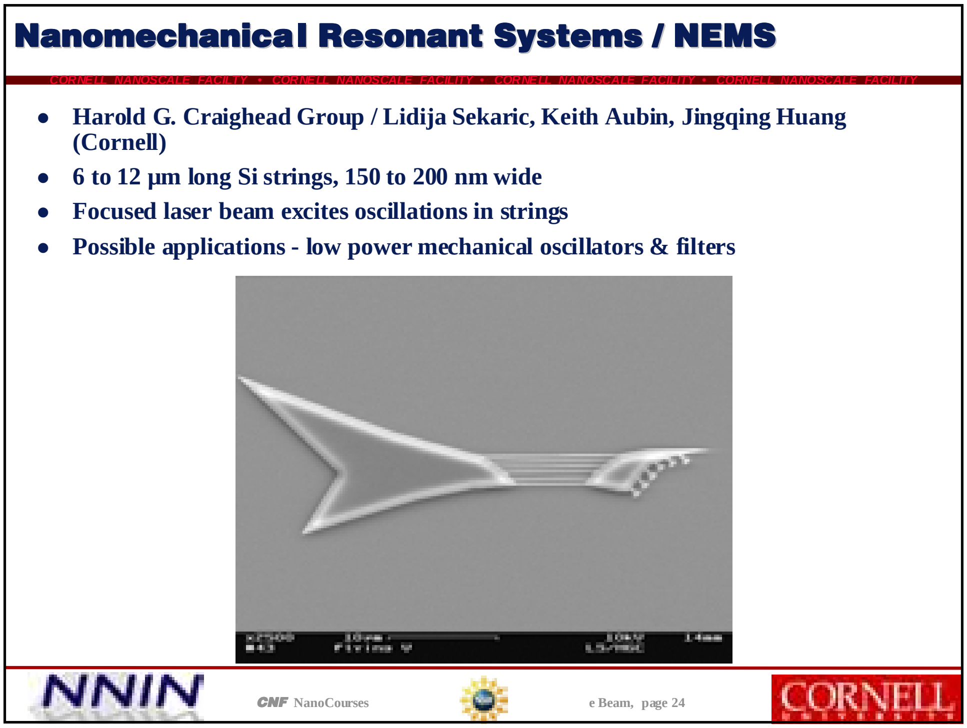
Studying Organic Semiconductor Molecules

- Yuanjia Zhang,George Malliaris (Cornell)
- 27 nm gap between electrodes



Nanomechanical Resonant Systems

- Harold. G. Craighead group / Dustin Carr (Cornell)
- Released silicon
- 50 nm strings on “harp”



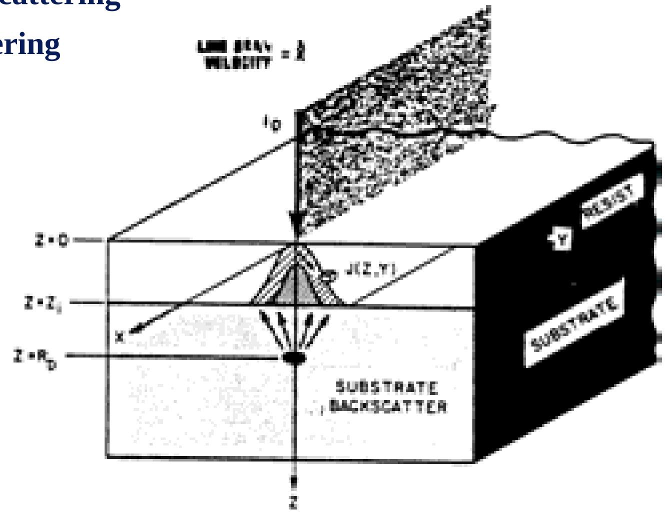
Nanomechanical Resonant Systems / NEMS

- Harold G. Craighead Group / Lidija Sekaric, Keith Aubin, Jingqing Huang (Cornell)
- 6 to 12 µm long Si strings, 150 to 200 nm wide
- Focused laser beam excites oscillations in strings
- Possible applications - low power mechanical oscillators & filters

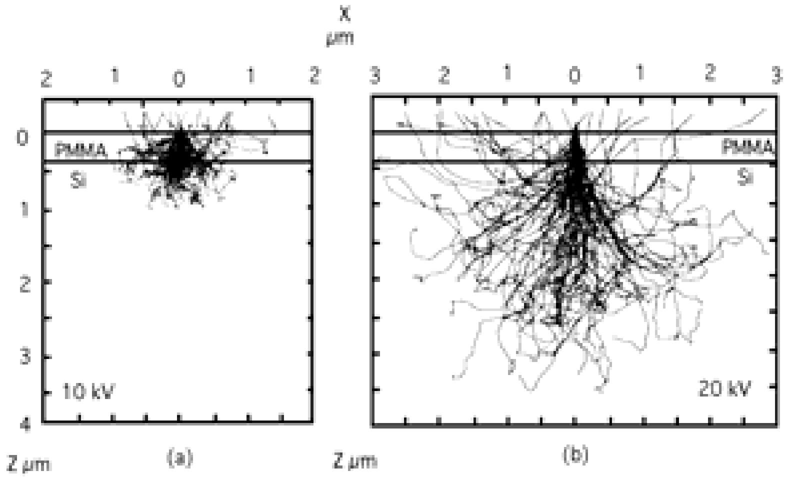
A Little Physics

Electron-solid interactions

- Forward scattering
- Backscattering



Electron Scatter Kernel

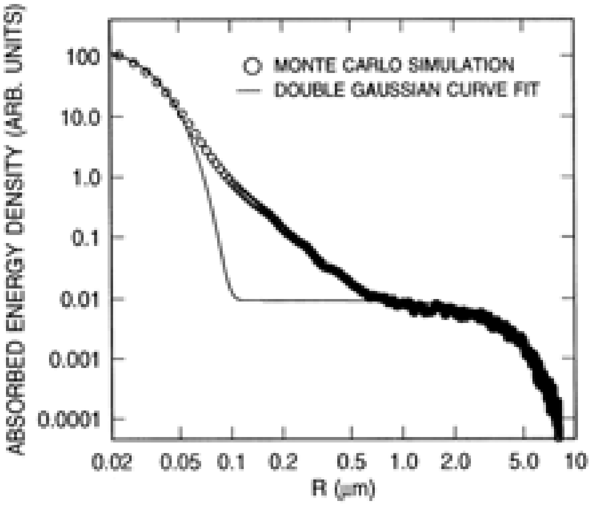


- SPIE Handbook of Microlithography, Micromachining and Microfabrication. Volume 1: Microlithography. P. Rai-Choudhury, ed. Ch. 2:Electron Beam Lithography, Mark A. McCord and Michael J. Rooks, 1997, p. 157

Secondary electrons

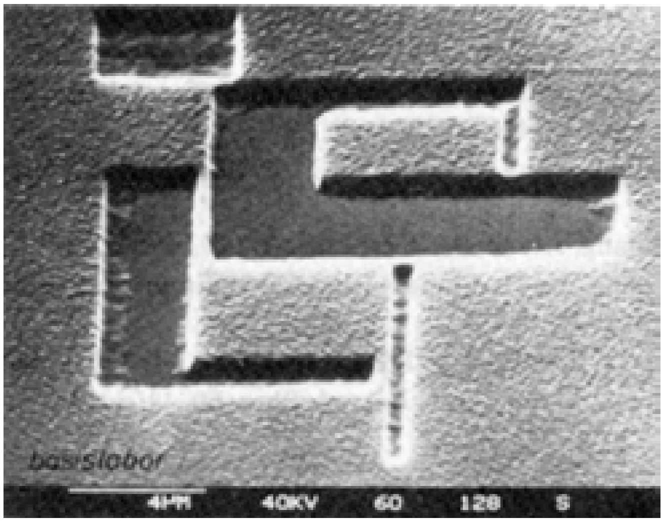
- Much of primary electron energy is dissipated in the form of secondary electrons with energies from 2 to 50 eV
- Responsible for the bulk of the actual resist exposure process
- Range in resist is only a few nanometers
  - Contribute little to the proximity effect
- Net result is effective widening of the beam by roughly 10 nm
- Main reason for minimum practical resolution of 20 nm in the highest resolution electron beam systems
- Contributes (along with forward scattering) to the bias that is seen in positive resist systems, where the exposed features develop larger than the size they were nominally written.

Modeling



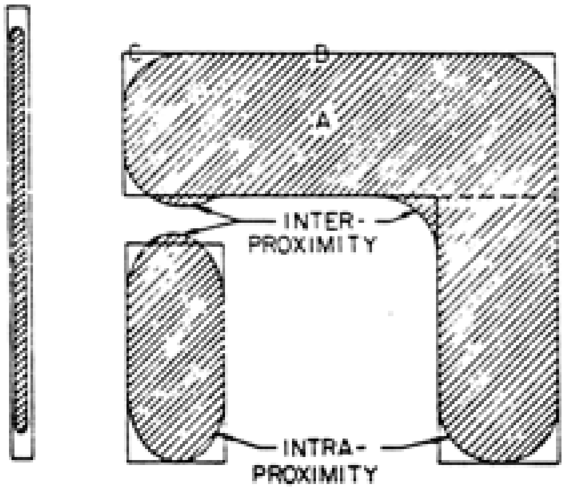
SPIE Handbook of Microlithography, Micromachining and Microfabrication. Volume 1: Microlithography. P. Rai-Choudhury, ed. Ch. 2:Electron Beam Lithography, Mark A. McCord and Michael J. Rooks, 1997, p. 158

Proximity effect



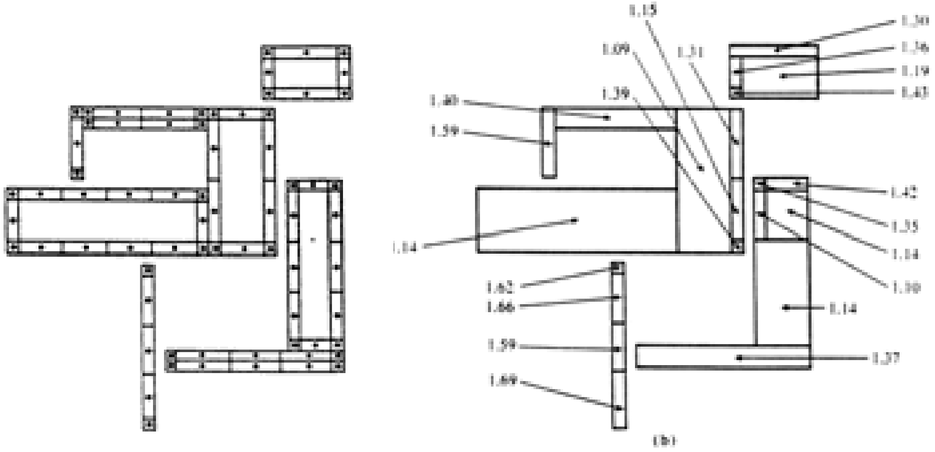
E. Kratschmer, “Verification of a proximity effect correction program in electron beam lithography,” J. Vac. Sci. Technol. 19 (4), 1264-1268, 1981, p. 1267

Proximity Effect – Inter- and Intra-



Conditional Feature Assignment with CATS

- Primitive proximity effect correction by assigning dose clocks to features of different sizes



Using e-Beams

- in the order you would actually do things

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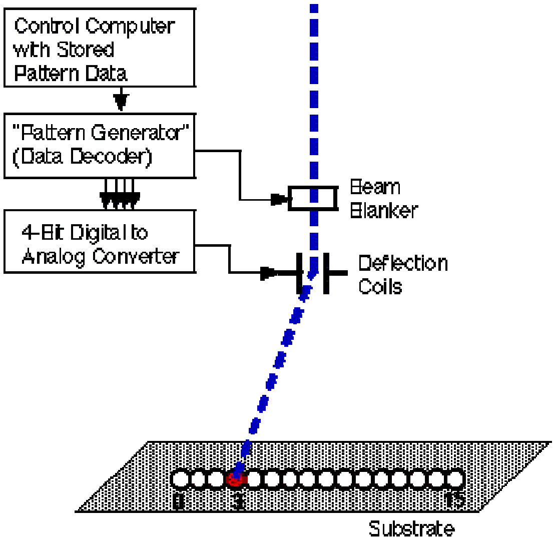
e-Beam Lithography Procedure

- Design Pattern with CAD
  - Convert Pattern to Machine Format
- Choose Resist and Apply to Sample
- Expose
- Develop

Background for CAD - Beam Scan Basics



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html

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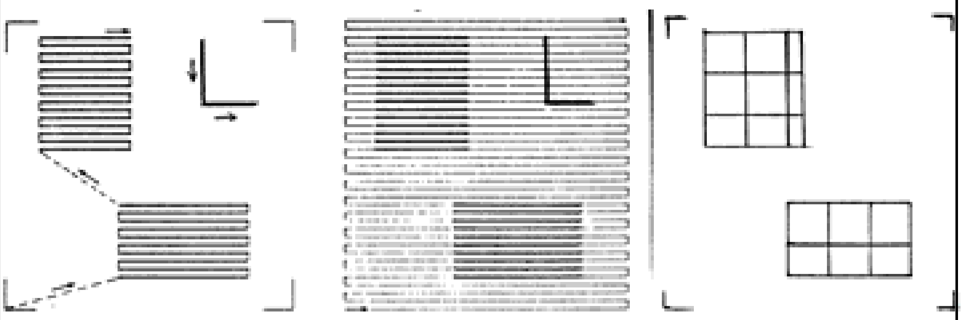
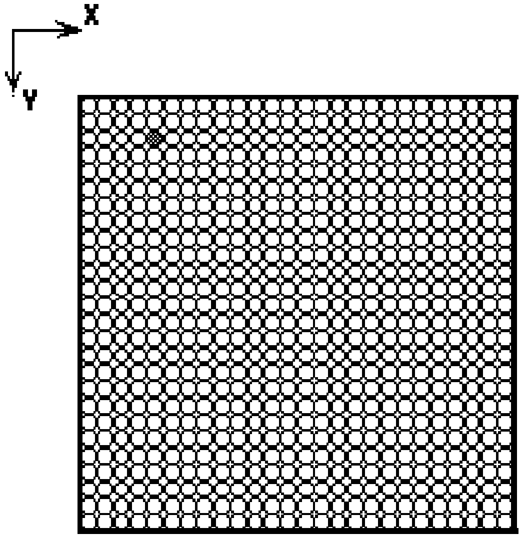
Pattern Writing Strategies

- Vector Scan
- Raster Scan
- Shaped Beam

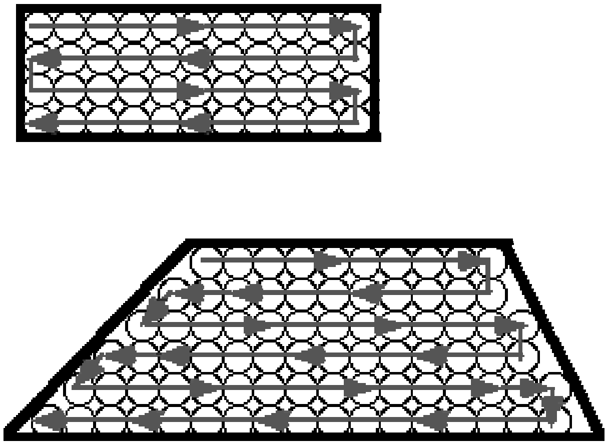


Two Dimensional e-Beam Field



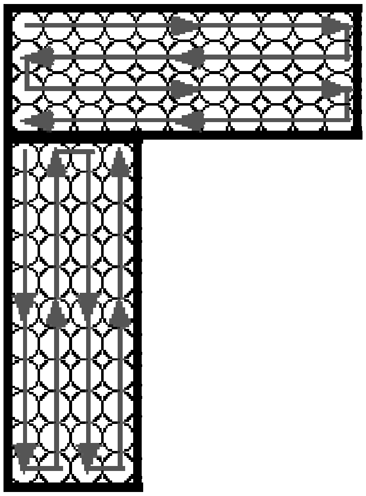
- Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html

Vector Scan to Fill In Shapes



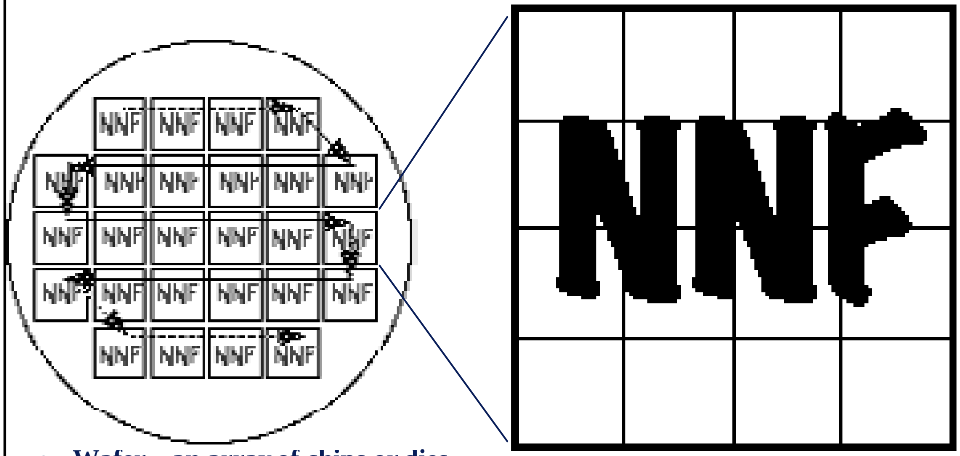
- Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html

Fracturing Shapes



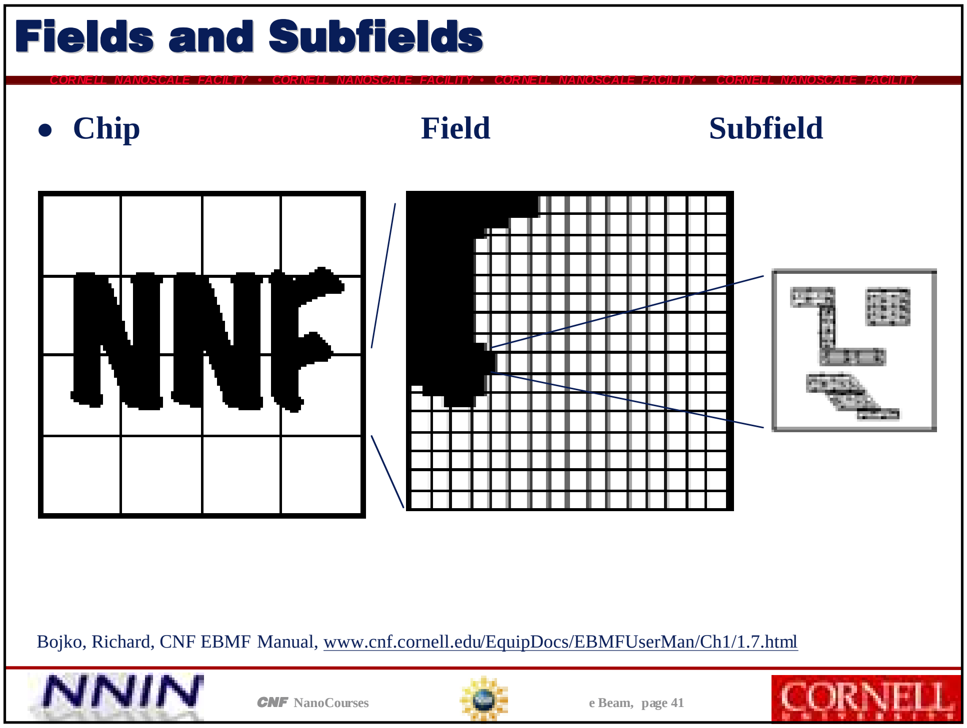
Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html

Hierarchy of Pattern Exposure Elements



- Wafer – an array of chips or dies
- Die or chip – one or more fields

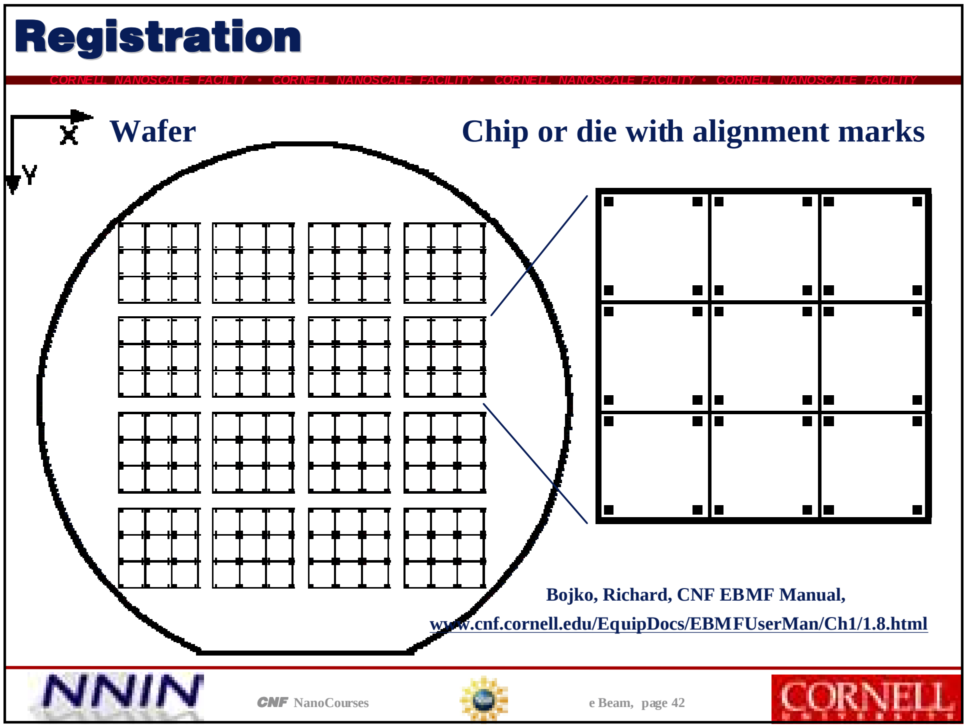
Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html



Fields and Subfields

- Chip Field Subfield

Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.7.html



Registration

Wafer **Chip or die with alignment marks**

Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch1/1.8.html

Resolution, Current and Dose Issues

- Dose is charge/area, $\mu C/cm^2$

$$D = \frac{I \times t}{A} = \frac{I}{A \times f}$$

- I = current, typically 1, 2, 5, 10, 20, 50 nA
- A = area for a single beam step, e. g. 5 nm x 5 nm
- f = clock frequency
- Higher current -> faster write time, but lower resolution
- Stage moves (~ 1 s) may be major contributor to exposure time

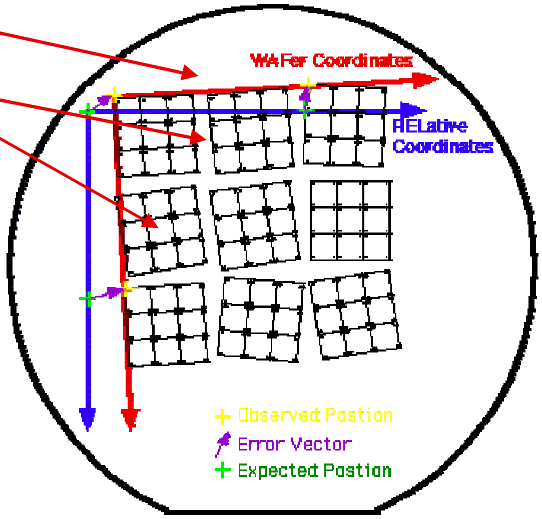
Variable Resolution Unit (VRU) table

- VRU is a multiple of smallest beam step size
- CFREQ command on VB6 calculates clock frequency, current, dose or exel (beam step) size
- Trade off current and beam step size to get high resolution and fast write time with less than max. clock frequency

VRU	Beam Step Size, nm	Min. Dose, uC/cm^2
1	5	160
2	10	40
4	20	10
8	40	2.5
16	80	0.63
32	160	0.16

Coordinate Systems / Stage Mapping Modes

- Global / Wafer
- Die / Chip
- Field within chip



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.5.html

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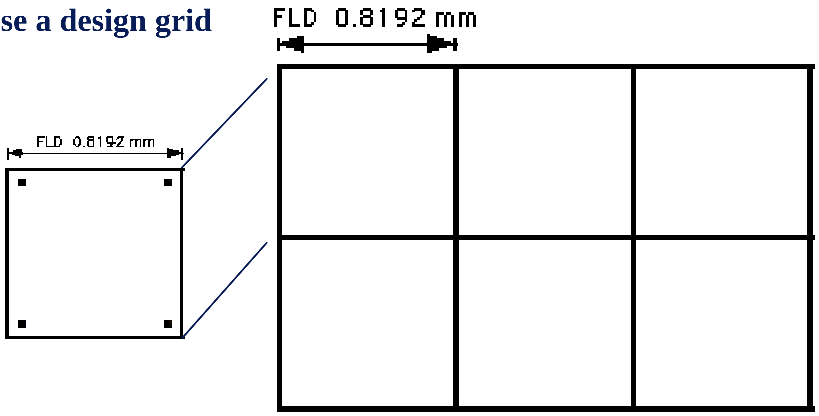
General Guidelines for Pattern Layout

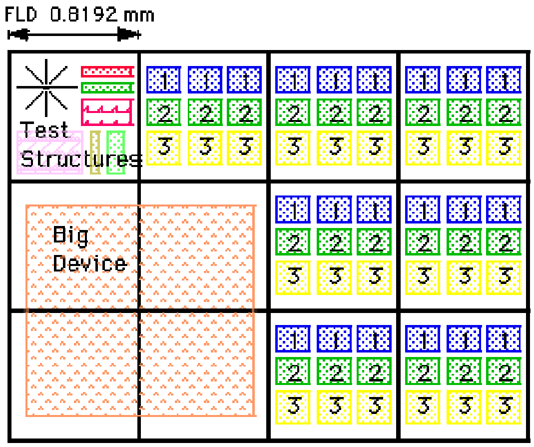
- Design for e-Beam exposure
- Use a design grid



Bojko, Richard, CNF EBMF Manual,
www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.5.html and
www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch2/2.3.html

Populated Grid

- No field stitching except in BigDevice which is larger than one field



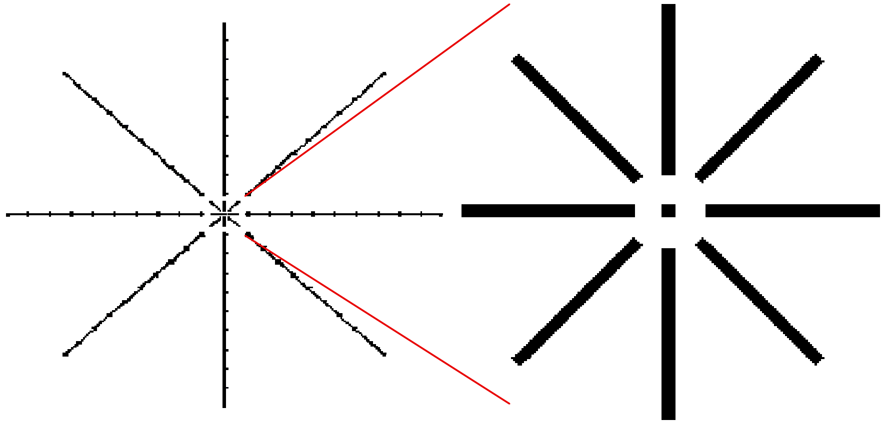
Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch2/2.3.html

Combining e-Beam with Other Types of Lithography

- Alignment accuracy ~ 10 nm is achievable
- Techniques that make alignment marks visible (to your eye *and* to the machine) in a 100 keV scanning electron beam include
    - Specific shapes
        - Squares or octagons with 4-50 µm sides
    - Materials
        - 1 µm-deep etched pits in Si
        - 50 - 100 nm of Au, Pt, W liftoff metal (high atomic number difference between mark and substrate)
        - Al doesn’t work on Si or GaAs substrates

Making and Positioning Marks

- Global marks
  - 3 widely spaced marks such as GCA key



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch2/2.3.html

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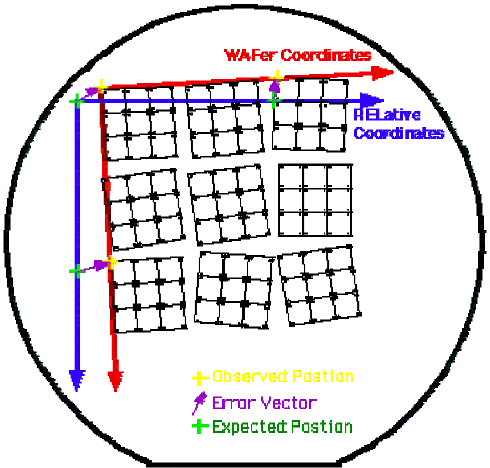
Locating Marks

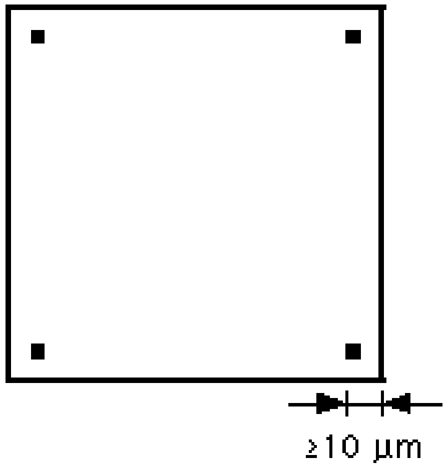
- Global Alignment or Wafer Alignment



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.5.html

Local or Field Alignment

- Typical 4 mark field



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.3.html

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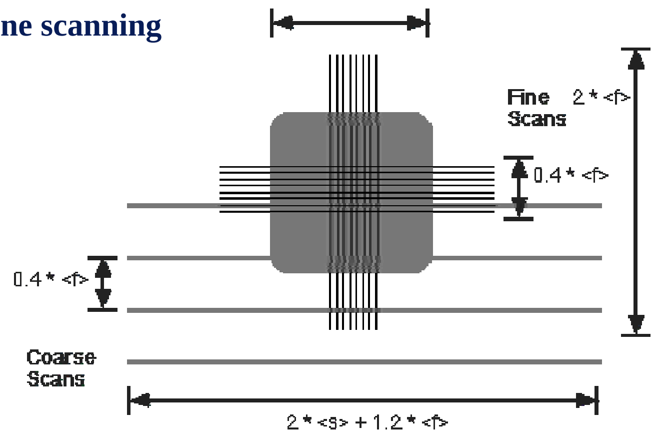
Basic Mechanisms of Alignment

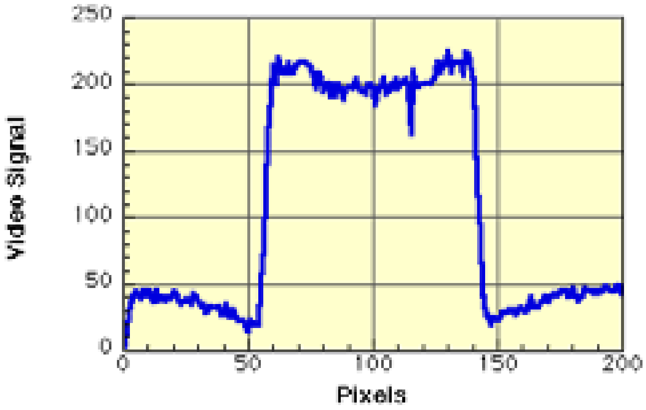
- Simple image processing
- Coarse and fine scanning



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.2.html

Easy Mark

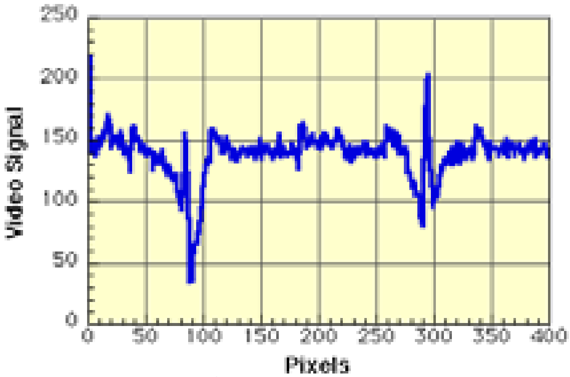
- **Hi Z contrast between Au mark on Si, no resist**
- **4 µm wide mark, 80 pixels wide**



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.1.html

Difficult Mark

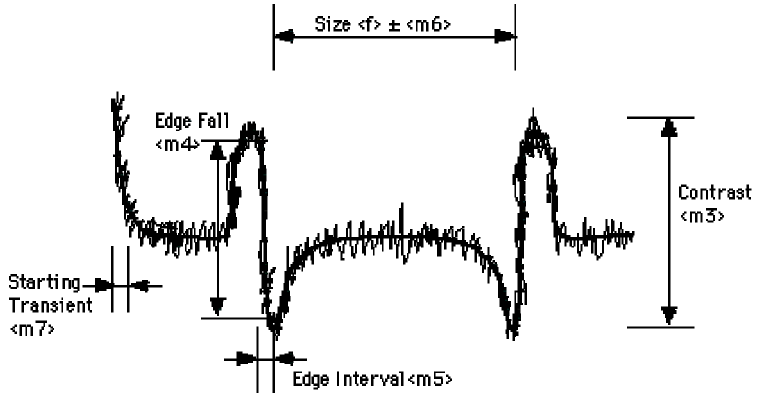
- **400 nm Tantalum on Si, buried under 100 nm thick SiO_2 film**
- **Only topographic edge contrast seen**
- **Noise from roughness of tantalum surface**



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.1.html

Mark Parameters

- Schematic line scan of a pit type alignment mark scan on EBMF



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.2.html

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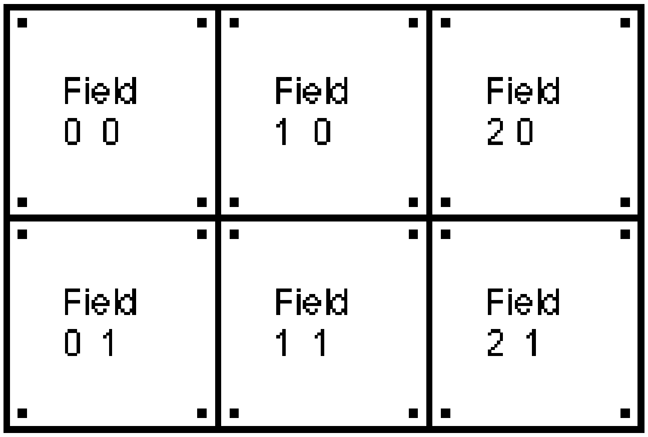
Multi-field Die Alignment

- Field by Field Alignment



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch6/6.8.html

Resists and Processing

- Positive resists
    - PMMA
    - Toray EBR-9
    - PBS
    - ZEP
    - Photoresists as e-beam resists
- Negative resists
    - COP
    - Shipley SAL
    - NEB-31
- Multilayer systems
    - Low/high molecular weight PMMA
    - PMMA/copolymer
    - Trilayer systems

Poly(methyl methacrylate) (PMMA)

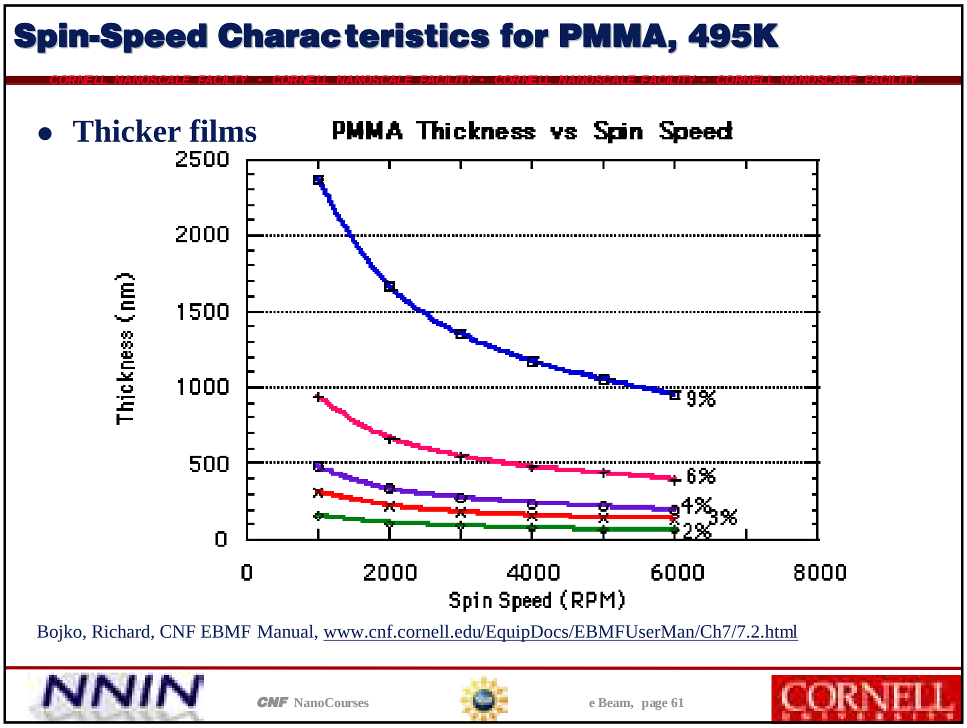
- The most popular e-Beam resist
- Extremely high-resolution
- Easy handling
- Excellent film characteristics
- Wide process latitude
- Usually dissolved in a solvent (e.g. anisole)
- Exposure causes scission of the polymer chains
- Solvent developer dissolves exposed (lighter molecular weight) resist

PMMA Characteristics

- Positive acting
- Several viscosities available, allowing a wide range of resist thickness
- Not sensitive to white light
- Developer mixtures can be adjusted to control contrast and profile
- Appropriate processing results in undercut profile for liftoff
- Poor dry etch resistance
- No shelf life or film life issues

PMMA Basic Processing

- Surface Preparation
  - In general, no surface preparation (aside from normal cleaning) is necessary. Excellent adhesion to most surfaces
- Spin
  - Speed 1000-5000 rpm, 60 sec. (100-1000 nm)
- Pre-bake
  - 170 deg C oven, 1 hr. Non-critical. Must be $150 < T < 200$ degrees, for at least 30 minutes. May also be hot-plate baked
- Expose
  - Dose around 100 $\mu C/cm^2$ at 20 kV

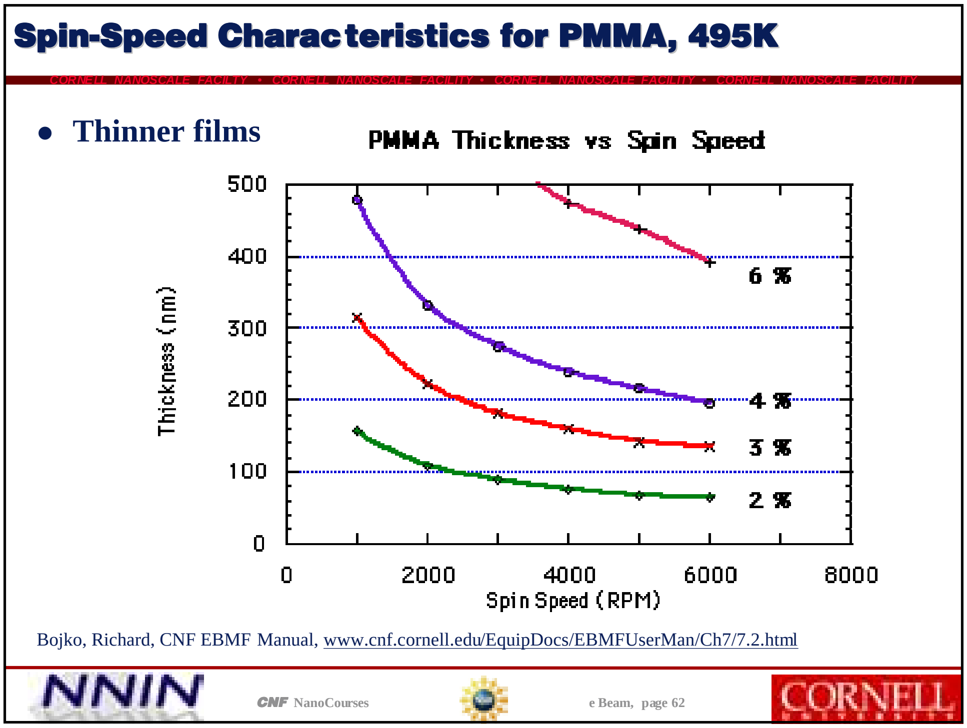


Spin-Speed Characteristics for PMMA, 495K

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

- Thicker films

Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch7/7.2.html



Spin-Speed Characteristics for PMMA, 495K

CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY • CORNELL NANOSCALE FACILITY

- Thinner films

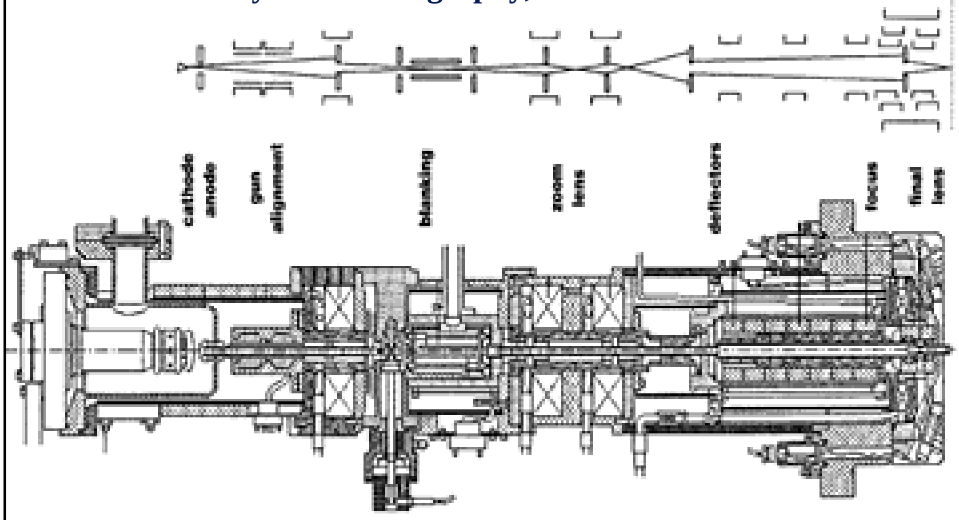
Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch7/7.2.html

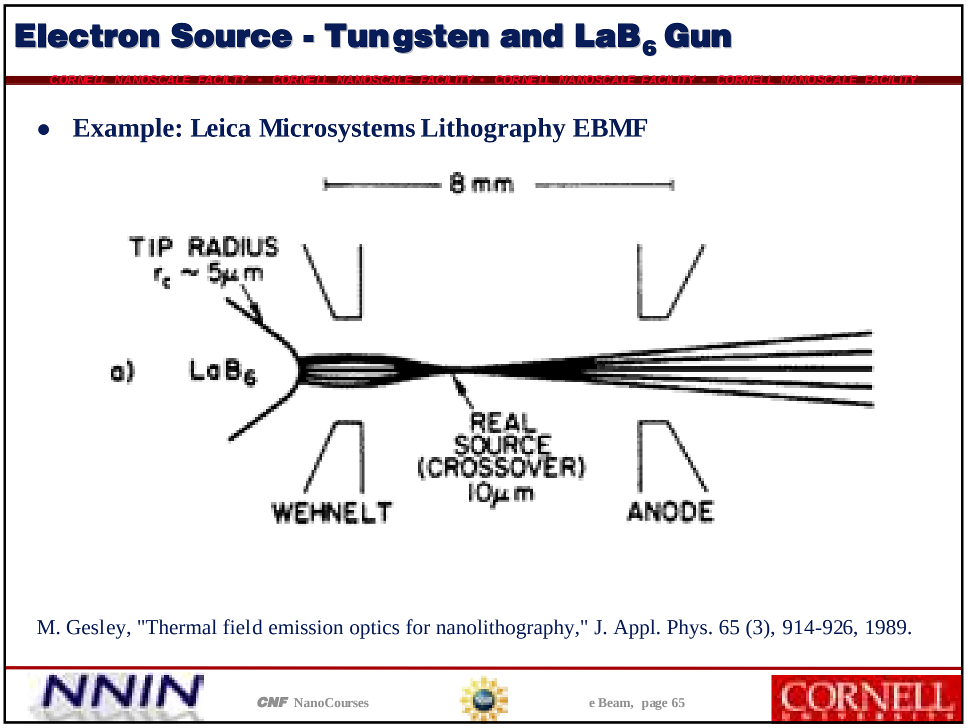
P(MMA-MAA) Copolymer Resist

- Higher sensitivity than PMMA
  - Can be exposed at a lower dose
  - Faster
  - Less contrast
- Most useful in Bi-level resists with PMMA, to produce undercut profiles useful in liftoff processing
- Characteristics
  - Positive acting
  - Several viscosities available, allowing a wide range of resist thickness
  - Not sensitive to white light
  - Developer mixtures can be adjusted to control contrast and profile
  - Poor dry etch resistance
  - No shelf life or film life issues

Tour through an e Beam Lithography Column

- **Leica Microsystems Lithography, Ltd. VB6**

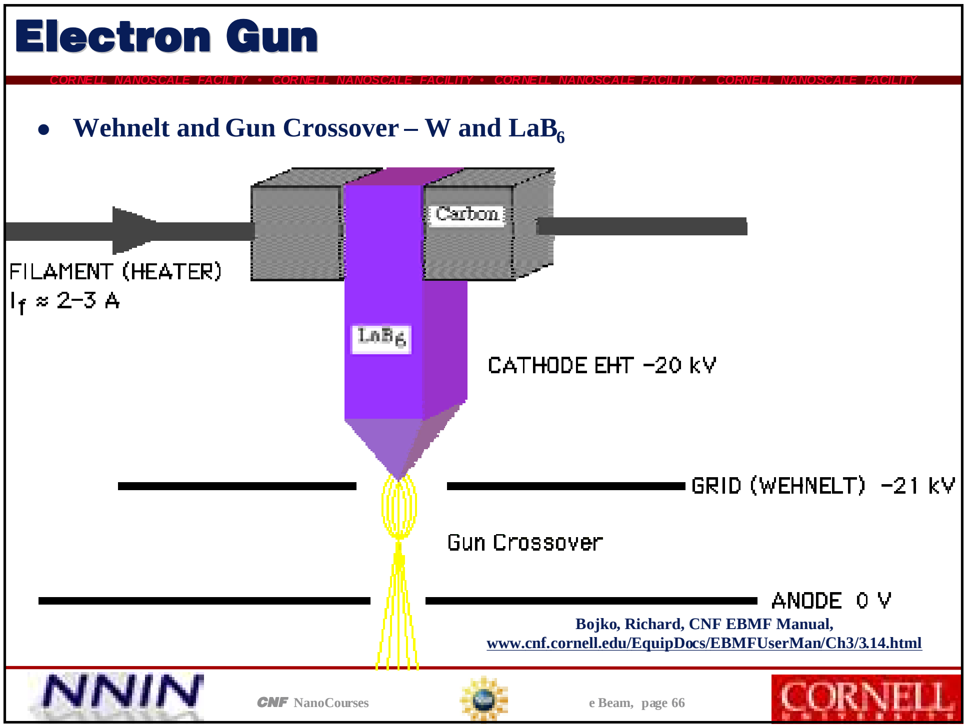




Electron Source - Tungsten and LaB$_6$ Gun

- **Example: Leica Microsystems Lithography EBMF**

M. Gesley, "Thermal field emission optics for nanolithography," J. Appl. Phys. 65 (3), 914-926, 1989.



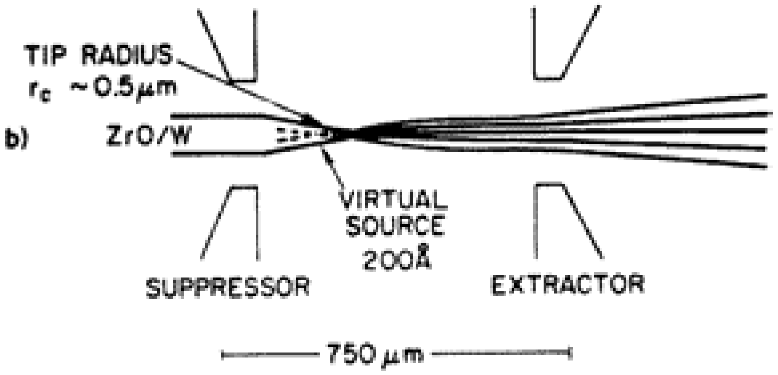
Electron Gun

- **Wehnelt and Gun Crossover – W and LaB$_6$**

Bojko, Richard, CNF EBMF Manual,
www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch3/3.14.html

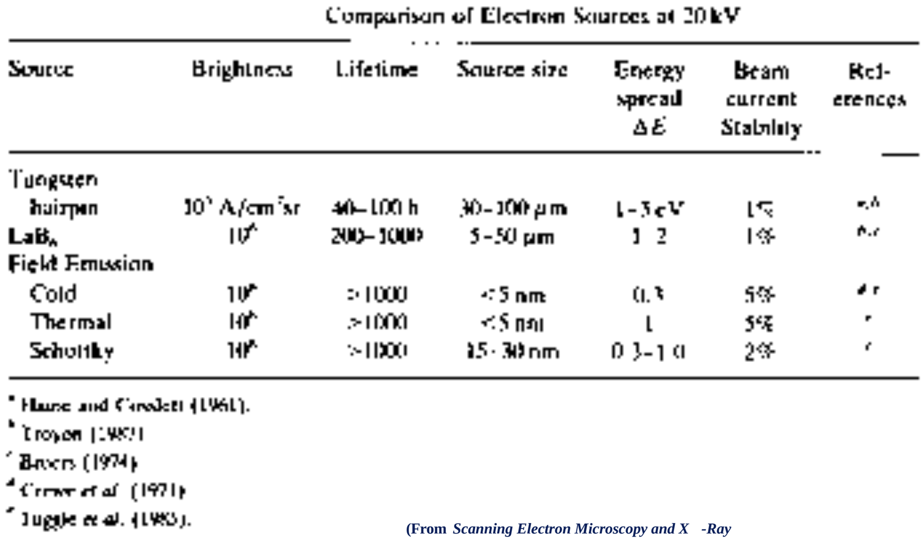
Electron Source – Thermal Field Emitter (TFE)

- Example: Leica Microsystems Lithography VB6



M. Gesley, "Thermal field emission optics for nanolithography," J. Appl. Phys. 65 (3), 914-926, 1989, p. 915

Comparison of Electron Sources



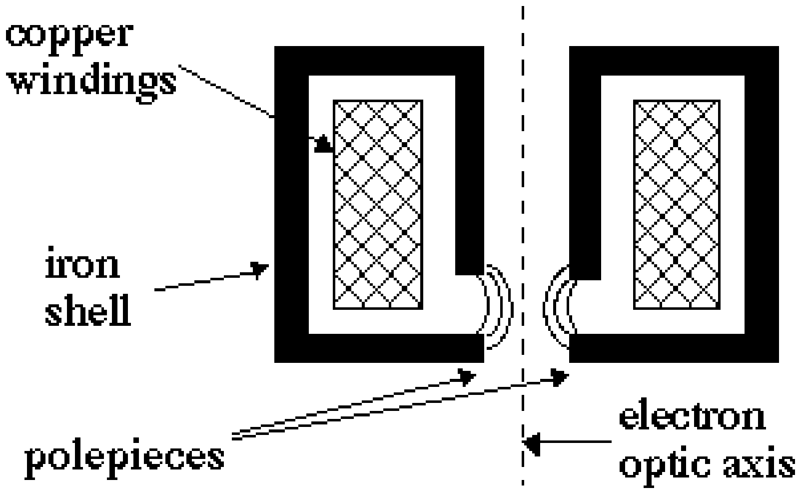
Comparison of Electron Sources at 20 kV

Source	Brightness	Lifetime	Source size	Energy spread ΔE	Beam current Stability	References
Tungsten						
hairpin	10^5 A/cm²sr	40–100 h	30–100 µm	1–3 eV	1%	a,b
LaB$_6$	10^6	200–1000	5–50 µm	1–2	1%	b,c
Field Emission						
Cold	10^8	>1000	<5 nm	0.3	5%	d,e
Thermal	10^8	>1000	<5 nm	1	5%	e
Schottky	10^8	>1000	15–30 nm	0.3–1.0	2%	e

[a] Haine and Cosslett (1961).
[b] Troyon (1987).
[c] Broers (1974).
[d] Crewe et al. (1971).
[e] Tuggle et al. (1985).

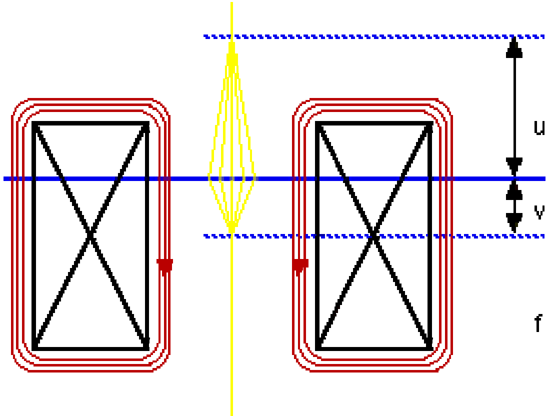
(From *Scanning Electron Microscopy and X -Ray Microanalysis* , Joseph I. Goldstein et al., Plenum Press)

Electron Optics – Magnetic Electron Lens



SPIE Handbook of Microlithography, Micromachining and Microfabrication. Volume 1: Microlithography.
P. Rai-Choudhury, ed. Ch. 2:Electron Beam Lithography, Mark A. McCord and Michael J. Rooks, 1997, p. 151

Magnetic Electron Lens



u = Object Distance

v = Image Distance

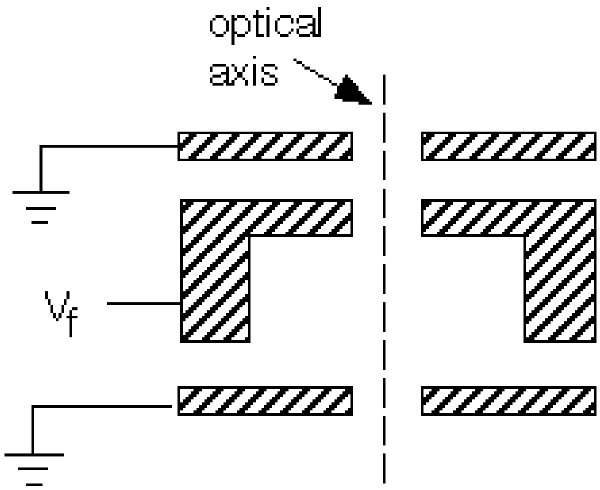
f = Lens Focal Length

Magnification: $m = \frac{v}{u}$

Simple Lens Equation: $\frac{1}{u} + \frac{1}{v} = \frac{1}{f}$

Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch3/3.13.html

Electrostatic Lens



SPIE Handbook of Microlithography, Micromachining and Microfabrication. Volume 1: Microlithography. P. Rai-Choudhury, ed. Ch. 2:Electron Beam Lithography, Mark A. McCord and Michael J. Rooks, 1997, p. 152

Other Electron Optical Elements

- **Beam blanking**
- **Stigmators**
- **Electron beam deflection**
- **Apertures**

Beam Blanking

- Turning the beam on and off
- Usually accomplished with a pair of plates set up as an electrostatic deflector
- One or both of the plates are connected to a blanking amplifier with a fast response time
- Voltage applied across plates sweeps beam off axis until it is intercepted by a downstream aperture
- *Conjugate blanking*
    - Beam at target does not move while the blanking plates are activated
    - Prevents leaving streaks in the resist as beam is blanked
    - Blanking plates are centered at an intermediate focal point, or crossover

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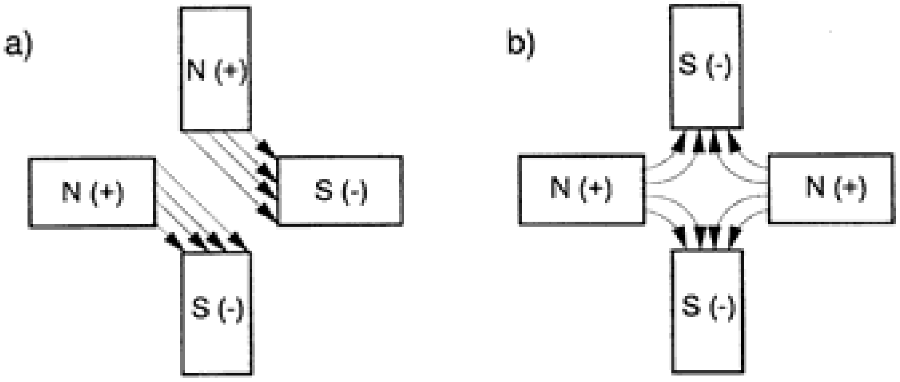
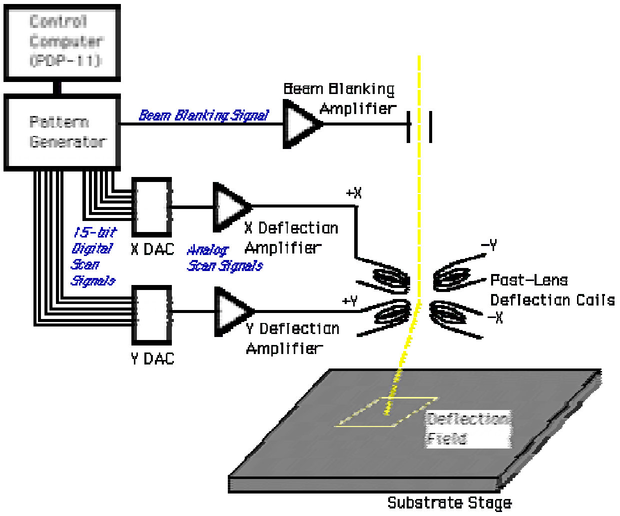
Deflector and Stigmator



SPIE Handbook of Microlithography, Micromachining and Microfabrication. Volume 1: Microlithography. P. Rai-Choudhury, ed. Ch. 2:Electron Beam Lithography, Mark A. McCord and Michael J. Rooks, 1997, p. 154

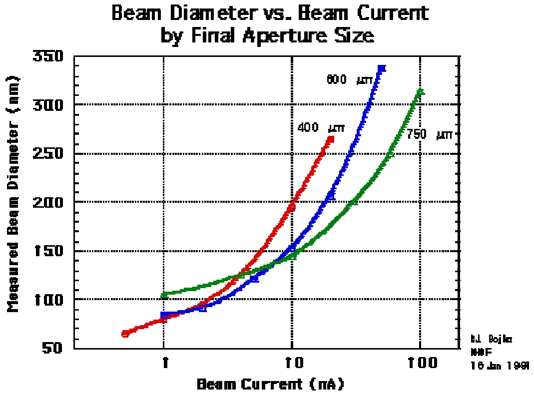
Beam Deflector



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch3/3.18.html

Final Aperture

- **Measured beam diameters at 20 kV**
- **Smaller final aperture does not always produce smaller beam**



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch3/3.16.html

Dynamic Corrections for Aberrations

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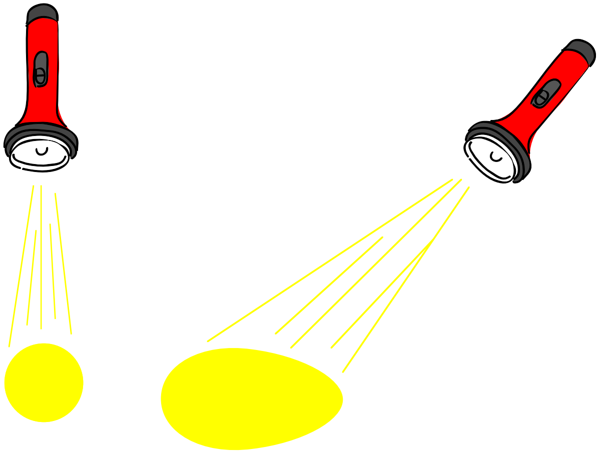
- Example: deflection-induced beam defocusing



Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch3/3.19.html

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Stage Enables sub-100 nm Lithography

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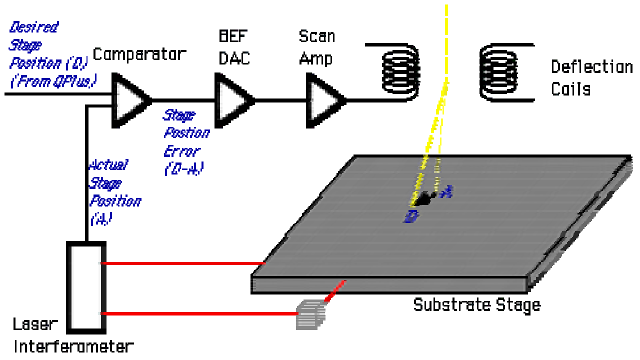
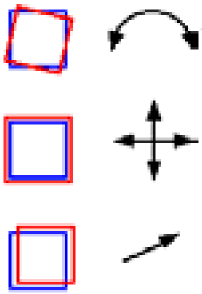
- Stage has laser interferometer with λ /1024 = 0.6 nm precision
- Beam Error Feedback (BEF) corrects for stage position and vibration in real time

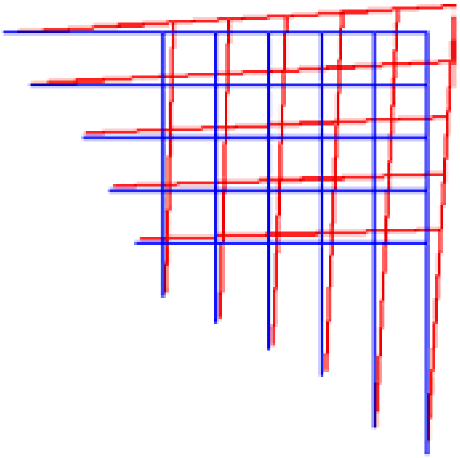


- Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch3/3.18.html

Mapping Distortions to Correct Them

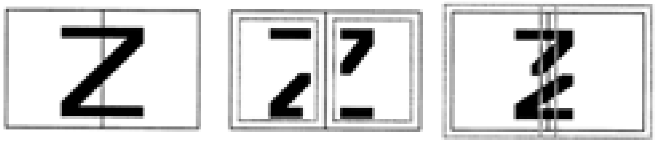
- Five coefficients parameterize distortion correction
  - Rotation Angle
  - X scaling
  - Y scaling
  - X translation
  - Y translation





Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.e

Height Mapping to Minimize Stitching Errors



In Focal Plane – OK Too High – Gap Too Low – Overlap

- Real time laser height sensor for dynamic correction of field size, focus, astigmatism

Bojko, Richard, CNF EBMF Manual, www.cnf.cornell.edu/EquipDocs/EBMFUserMan/Ch3/3.22.html

Typical Exposure Sequence

- Ready the airlock for venting
- Vent the airlock
- Load the wafer into a chuck
- Load the chuck into the airlock
- Pump the airlock back to vacuum
- Load and settle the chuck on the exposure stage
- Set up the machine operating parameters
- Run your exposure job file
- Unload chuck
- Remove the chuck from the airlock

PMMA Basic Processing – post exposure

- Develop
  - 1:1 MIBK:IPA, 1-2 minutes
- Rinse with IPA
- Dry by spinning or dry N_2
- Post-Bake not normally necessary
- Light Descum
- Stripping
  - Acetone will strip PMMA
  - NMP (Remover 1165)
  - Strong bases (KOH)
  - Acid normally hostile to organics, such as NanoStrip
  - Oxygen plasmas etch PMMA very well

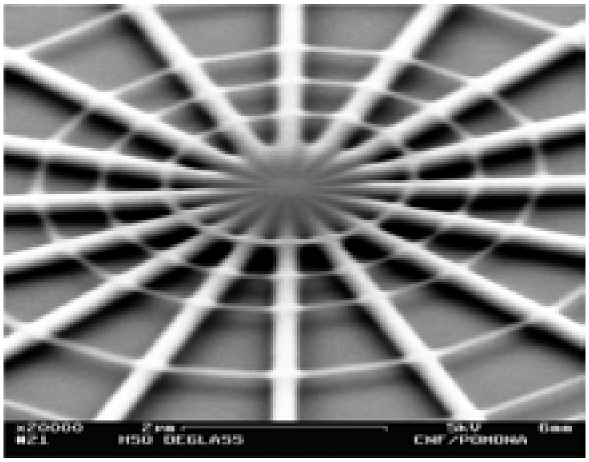
CNF e-Beam Systems

CNF has 3 complementary systems

1. Nabity Nanometer Pattern Generation System (NPGS) on LEO SEM
2. Leica VB6 HR
3. JEOL 9300FS

Nabity Nanometer Pattern Generation System (NPGS)

- PC-based pattern generator
- Interfaced to a LEO 982 scanning electron microscope
- 1 to 30 keV



David Tanenbaum
(Pomona College)

Leica VB6-HR

- For features from above 1 µm to below 30 nm
- Thermal Field Emission electron source running at 100 kV provides high brightness and small source size
- Minimum feature sizes < 30 nm are possible
- Field sizes up to 655 µm
- Beam currents as high as 50 nA
- Flexible job control language

JEOL 9300FS

- **General purpose high-resolution electron-beam lithography**
- **Thermal Field Emitter electron source at 100 kV**
- **Beam spot size 4 nm**
- **Repeatable minimum resolution < 20 nm**
- **Pixel step 1 nm**
- **Placement and automated alignment accuracies of 20 nm over a 0.5 mm field**
- **Max 25 MHz clock, 20-bit pattern generator**
- **Wafers and masks up to 12 inches**
- **Upgrades to 50 MHz clock and 1 mm field size in future**

References and Acknowledgements

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