D-Band Filters and Splitters Based on SiC Substrate-Integrated Waveguides

CNF Project Number: 3078-23
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Primary Source(s) of Research Funding:

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Primary CNF Tools Used: ABM Contact Aligner, SÜSS MA6-MB6 Contact Aligner, AJA Sputter Deposition - 1 & 3, AJA Ion Mill, Electroplating - Au & Ni

Abstract:

The objective of this project is to demonstrate the feasibility for monolithic integration of antennas, filters, and high-electron mobility transistors (HEMTs) on SiC. To demonstrate that individual components survive the monolithic integration, the D-band filters based on SiC substrate-integrated waveguides (SIW) are designed, fabricated, and measured. The resulted D-band (110.170 GHz) SIWs exhibit a record low insertion loss of 0.22 ± 0.04 dB/mm, which is four times better than that of the GCPWs. A 3-pole filter exhibits a 1.0-dB insertion loss and a 25-dB return loss at 135 GHz, which represents the state of the art of SiC SIW filters and is order-of-magnitude better than Si on-chip filters. The compact filters are designed, fabricated, and measured but exhibit high insertion loss due to the high resistance of the through-substrate vias (TSVs). Solid TSVs can minimize the resistance of the TSVs and thus decrease the insertion loss. The new process is under development and optimization. The D-band splitters are designed and will be fabricated and measured.

Summary of Research:

SiC SIWs are attractive because high-power and high-efficiency GaN amplifiers are usually fabricated on SiC. SiC is high in dielectric constant, electrical resistivity, breakdown strength, mechanical toughness, and thermal conductivity, but low in loss tangent and thermal expansion coefficient. Previously, for proof of principle, we used the custom process at Cornell University to design and fabricate a 3-pole filter comprising three SIW resonators, which exhibited a 1-dB insertion loss and a 25-dB return loss at 135 GHz [1]. These record performances (Table I and Table II) make SIW promising for monolithic integration of high-quality SIW filters, edge-firing SIW antennas, and GaN HEMTs as shown in Figure 1.

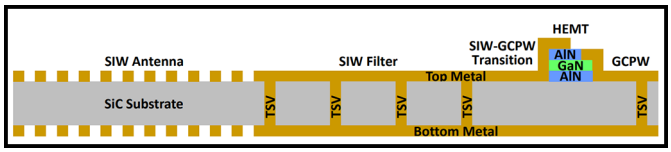

Figure 1: Schematics of an MMIC with an edge-firing SIW antenna, an SIW filter, and a GaN HEMT on the same SiC chip.

The first custom process is using Ni/Al as the top and bottom metal because of the limitation of the CNF tools. On the other hand, sidewalls of the TSVs are covered by sputtering Al. To further reduce the conductor loss, Au was used to replace the Al as the bottom metal. The Au is deposited planetary evaporation to cover the sidewalls of the TSVs. Since the depth of the TSV is 100 μm while the TSV diameter is 50 μm, the Au cannot cover the TSVs due to such high aspect ratio as depicted in Figure 2. The solid TSVs by electroplating Au could solve this issue but needs better control of the ICP-RIE etching of the SiC substrate. The etching recipe has been successfully transferred to Notre Dame.

In addition to the changes in metal, 4" SiC wafers are replacing the small chips (1 cm by 1 cm). The hard mask is critical for the ICP-RIE etching. Ni is the typical choice with the high selectivity and simple process. The SiC substrate is 100 μm in thickness which requires at least 3.3-μm thick Ni hard mask. In the first custom process, pure Ni was sputtered on small chips as the seed layer for Ni electroplating. When handling the 4" SiC wafers, the pure Ni seed layer cannot sustain such high stress strength from the 3.3-μm Ni. The combination of Ti and Ni can bear high stress strength from the thick Ni. The potential problem along with Ti is that Ti is hard to get removed thoroughly and if it's the case, the following ICP-RIE etching will fail and the whole wafer will be useless.

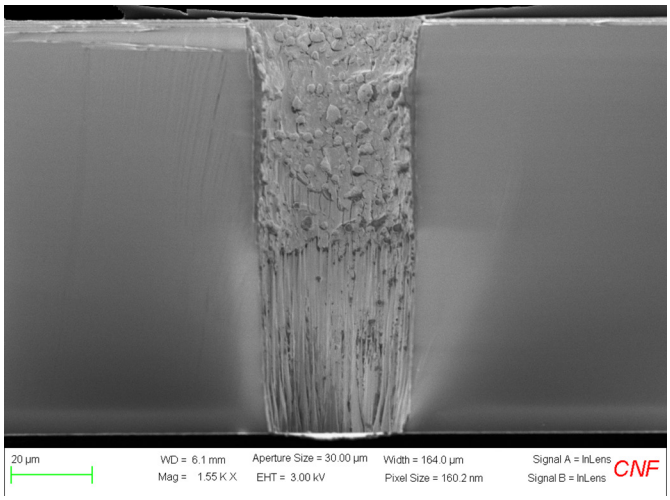

Figure 2: SEM image of the cross-section of the TSV after Au planetary evaporation.

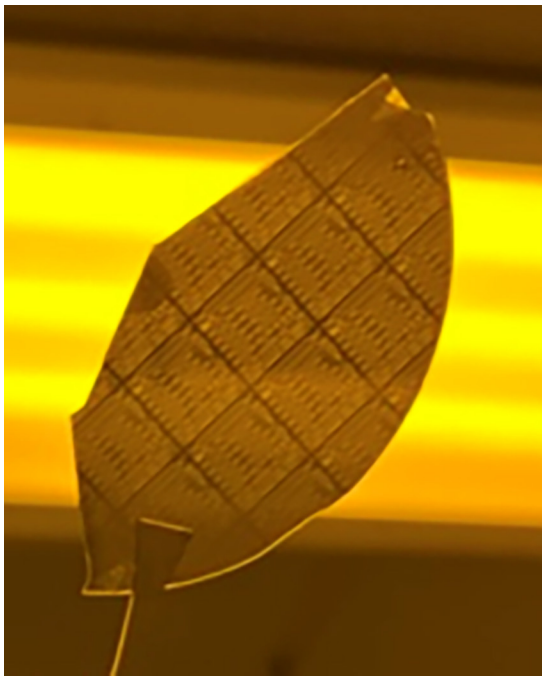

Figure 3: SiC test chip after ICP-RIE etching.

The test has been performed with the sequential processes of Ti/Ni seed layer sputtering, Ni hard mask electroplating, Ion mill, and then ICP-RIE etching. The results have proved that Ti will not affect the SiC etching as shown in Figure 3.

Conclusion and Future Steps:

The compact filters are designed, fabricated, and measured exhibiting high insertion loss due to the high resistance of TSVs. The new process on 4" SiC wafers are under development using Au for top and bottom metal layer, solid TSVs by electroplating Au. Meanwhile, the D-band splitters are designed. The new masks including filters and splitters are prepared. Each individual process has been validated except the Au electroplating on the 4" SiC wafers.

The new run of fabrication has started and will move on if the tools in CNF work well. The Au electroplating will be verified. The measurement will be performed in HFTL (Bard 315) using the 220 GHz single-sweep probe station system at Cornell University and banded probe station system in University of Notre Dame, respectively, for cross check and validation.

References:

[1] M. J. Asadi, L. Li, K. Nomoto, Y. Tang, W. Zhao, P. Fay, D. Jena, H. G. Xing, and J. C. M. Hwang, "SiC Substrate-Integrated Waveguides for High-Power Monolithic Integrated Circuits Above 110 GHz," 2021 IEEE MTT-S Int. Microw. Symp. (IMS), Atlanta, GA, USA, 2021, pp. 669-672.