Developing a Passivation-First Recessed T-Gate Procedure for AlN/GaN/AlN HEMTs

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Principal Investigator(s): Austin Hickman
User(s): Austin Hickman, Shankar Miller-Murthy

Affiliation(s): Soctera Inc.

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Contact: austin.hickman@soctera.edu, shankar.murthy@soctera.com

Primary CNF Tools Used: I-line stepper, PT770 Etcher, Oxford 81 Etcher, Odd hour E-beam evaporator, JEOL 6300 EBL, Oxford PECVD, AJA Sputter Deposition, Woolam Ellipsometer, Zeizz Ultra SEM, Leica Critical Point Dryer, Glen1000 resist stripper, P7 profilometer

ELECTRONICS

Abstract:

In this work, we report functional recessed T-gate structures fabricated using a procedure compatible with the AlN/GaN/AlN structure. The devices were fabricated on an AlGaN/GaN chip using a combination of gentle fluorine-based plasma etching and a buffered oxide etch (BOE) wet process to selectively remove passivation without implanting fluorine-based trap states. The devices demonstrated on-currents over 1.15 A/mm with an on-resistance of 1.8 Ω·mm. Transfer characteristics revealed I_{on}/I_{off} ratio of 10^4 and peak transconductance of 0.3 S/mm.

Summary of Research:

Next-generation (6G) wireless communication and high-resolution radar systems target high-power operation in the terahertz regime. Gallium nitride high-electron-mobility transistors (GaN HEMTs) are well-suited for this high-power, high-frequency application. However, the conventional AlGaN/GaN heterostructure provides poor quantum confinement of the two-dimensional electron gas (2DEG), generating short channel effects at high frequencies. Additionally, its RF power performance is limited by the breakdown voltage. The AlN/GaN/AlN heterostructure offers material and device design advantages over the conventional AlGaN/GaN HEMT: the AlN buffer tightly confines the 2DEG and offers a higher thermal conductivity path than a thick GaN buffer, and the AlN barrier induces higher density 2DEGs at thinner distances (5 nm). AlN also maximizes the barrier bandgap, improving breakdown voltage.

Recently, fully realized T-gated AlN/GaN/AlN HEMTs were fabricated and characterized. The T-gates were defined via two-stage electron beam lithography using a single followed by a double-layer resist stack. The first single-layer resist was used to define the gate stem combined with a chrome mask layer to ensure vertical side-walls, which was etched out of the SiN passivation using a combination of SF_4 plasma etching and a single minute of buffered oxide etch exposure to remove the last remaining SiN and expose the AlGaN without implanting any ions. The resulting structure is shown in Figure 1. The second, double-resist electron beam lithography exposure was used to define the head area, where Ni/Au (50/200 nm) gate metal was deposited via e-beam evaporation. The resulting structure is shown in Figure 2.

The devices demonstrated on-currents over 1.15 A/mm with an on-resistance of 1.8 Ω·mm. Transfer characteristics revealed I_{on}/I_{off} ratio of 10^4 and peak transconductance of 0.3 S/mm. All DC characteristics are shown in Figures 3 and 4.

These positive results, even at this early stage of the project, illustrate the effectiveness of this technique. With some refinement, it may allow the AlN platform to enable the next generation of high-power, mm-wave communication.

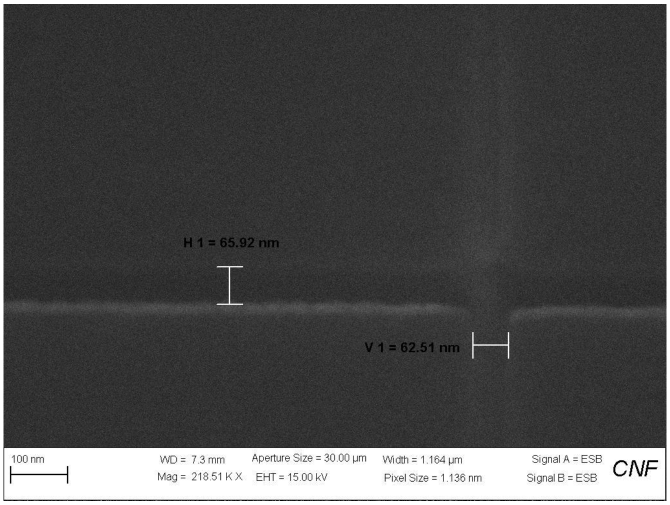


Figure 1: T-gate stem trench demonstrating a gate length of 65 nm.

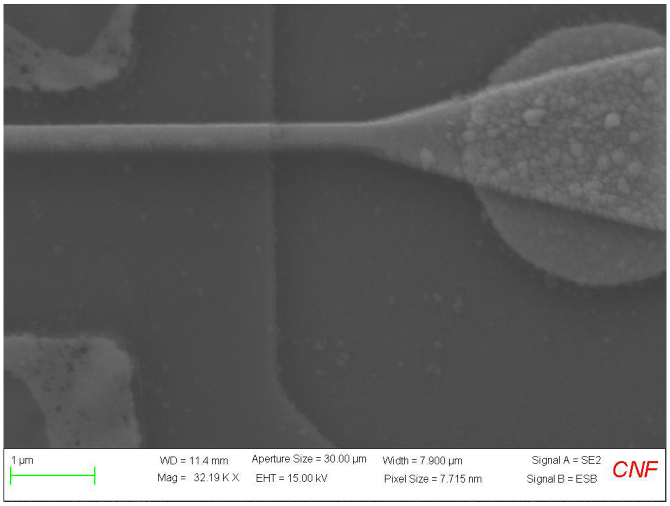
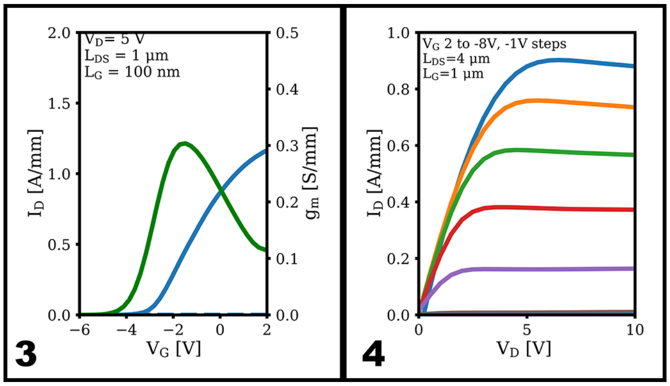


Figure 2: T-gate head with buried trench demonstrating a gate head width of ~250 nm.



Figures 3 and 4: DC characteristics for AlGaN/GaN recessed T-Gate HEMT.