HF Vapor Release Etch

CNF Project Number: 1611-07
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Primary Source(s) of Research Funding: National Science Foundation

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Primary CNF Tools Used: Primaxx Vapor HF Etcher

Abstract:

Reversible computing reduces the energy dissipation of a circuit by using logical reversibility and quasi-adiabatic transitions, introducing a trade-off between energy and speed. Adiabatic CMOS is the most developed implementation of reversible computing, but it is ultimately limited by passive power, the energy dissipation caused by leakage. New computing approaches try to eliminate the leakage current completely by using micro-electro-mechanical systems (MEMs) as relays to implement computing. Unlike CMOS circuits, the MEMs relays do not have a subthreshold current since they have no electrical contact when they are off. However, the relays will wear out over time primarily due to degradation of the current-carrying contacts. Adiabatic Capacitive Logic (ACL) was proposed by Pillonnet and Houri as a novel approach to reversible computing that eliminates leakage current and does not have make and break contacts therefore avoiding the degradation problem seen in relays. The fabrication of these nano-relays requires a release etch to free the MEMs structures. A wet etch process with critical-point drying gave a very low yield, so a vapor HF process at the Cornell NanoScale Facility (CNF) was used instead.

Summary of Research:

The basic structure is shown in the diagram of Figure 1 in cross section. A control voltage is applied between the plates on the left side which pulls down the upper plate, changing the capacitance of the output capacitor at the right. A key step in the process is a vapor hydrofluoric acid (HF) release etch, performed at CNF using the Primaxx Vapor HF Etcher, instead of the liquid HF followed by critical point drying that we used previously. This greatly increased the yield of process, since the critical point dryer was a very difficult process to control, and nearly all devices would stick to the surface during the drying process. With the vapor process the yield increased to about 50% in the first two runs. One disadvantage of the vapor HF process is that the vapor etches the TiN electrode layer more than in a liquid HF process. This resulted in an increased access resistance between the probe pads and the device that adversely impacted the capacitance measurements.

An SEM micrograph of the finished device is shown in Figure 2. There is still some residual stress in the polysilicon layer that causes the springs to bend out of plane. During the fabrication the samples are given a high-temperature treatment after the polysilicon deposition that is intended to relieve stress in the film, but this process needs further optimization. Initial measurements show that the devices operate correctly, and the characteristics of the devices are being measured. A pull-in voltage at an average of 22V is observed, in close agreement with COMSOL simulations.

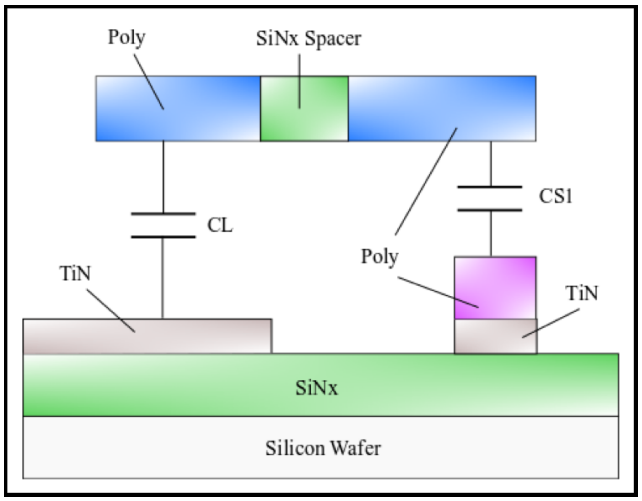

Figure 1: Voltage-controlled variable capacitor gap closing structure.

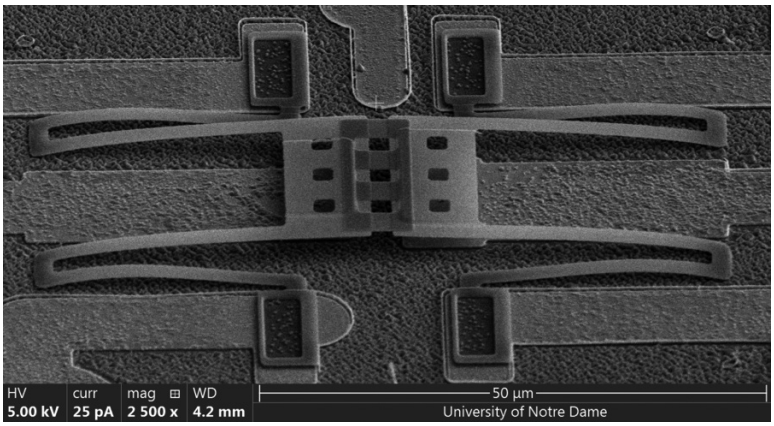

Figure 2: SEM micrograph of completed ACL variable capacitor.