Intrinsically Switchable Gigahertz Ferroelectric ScAlN SAW Resonators

CNF Project Number: 1121-03
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Primary Source(s) of Research Funding: Defense Advanced Research Projects Agency (DARPA) Tunable Ferroelectric Nitrides (TUFEN)

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Primary CNF Tools Used: SÜSS MA-6 Contact Aligner, CVC SC-4500 Odd-Hour Evaporator, JEOL 6300 Electron-Beam Lithography, Zeiss SEM

Abstract:

This work details intrinsic switching of 1-3 gigahertz (GHz) ferroelectric scandium aluminum nitride (ScAlN) surface acoustic wave (SAW) resonators. Reversible switching is demonstrated for SAW devices fabricated on 22-30% ScAlN, with metal interdigitated transducers (IDTs) of widths 1 µm-400 nm patterned with a combination of contact and electron-beam lithography. Two-state switching of the resonator is demonstrated with single-sided pulses of ± 6 MV/cm, which demonstrates reversible on-off switching of piezoelectricity in ScAlN. The results show a method of programmable RF signal processing and sensing using ferroelectric ScAlN.

Summary of Research:

Aluminum nitride (AlN) is used in MEMS RF resonators due to its excellent piezoelectric properties and CMOS-compatible processing. Fundamental limits in the piezoelectric properties of AlN have necessitated the exploration of new materials with improved performance. One such material is scandium aluminum nitride ($Sc_xAl_{1-x}N$), which can increase the piezoelectric coefficient by up to ~ 4x with Sc-incorporation. More recently, the discovery of ferroelectric switching in high Sc-concentration $Sc_xAl_{1-x}N$ (x>0.22), has generated significant interest as the first III-V ferroelectric [1].

To demonstrate reconfigurable and adaptive filtering, it is desirable to achieve programmable piezoelectric coupling in ScAlN with ferroelectric switching, which can then be used to tune the filter frequency and transmission level. We have previously reported on the ferroelectric properties of various ScAlN compositions across a range of device sizes, templating electrodes, film stress, and frequency of switching with a goal of identifying reduced switching voltages, including a reduction in the coercive field by 37% with *in situ* ovenization [2,3]. This work builds on the materials characterization and development we have performed previously by demonstration intrinsic polarization switching in ScAlN resonators [4].

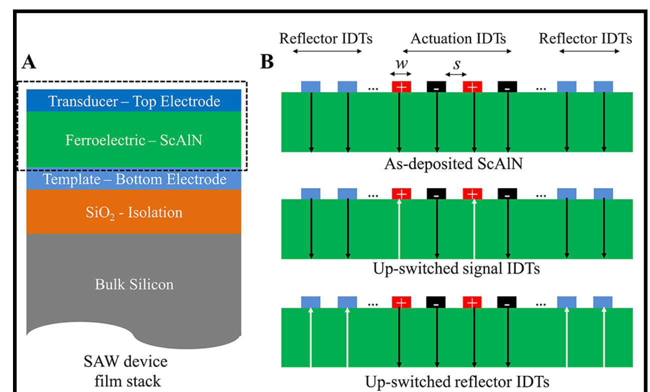

Figure 1: A) SAW device consisting of SiO_2 isolation, template bottom electrode, wurtzite ferroelectric ScAlN, and top electrodes for SAW actuation. B) Schematic of the transducer IDTs and ferroelectric ScAlN showing three distinct configurations of ScAlN polarization: as-deposited N-polar ScAlN with polarization pointing downward, up-switched ScAlN under signal IDTs to program piezoelectric coupling in the active region, up-switched ScAlN under reflector IDTs to program acoustic wave boundary conditions.

The film stack used to make the resonator comprises of a continuous bottom electrode which serves as the template for the ferroelectric, c-axis wurtzite ScAlN and the top electrode for patterning the SAW IDTs (Figure 1A). The IDTs with width w and spacing s enable lithographic definition of the resonance wavelength: $\lambda = 2(w+s)$. Passive reflectors enable energy confinement in the acoustic cavity defined by the IDTs. It is, hence, possible to switch the polarization of ScAlN under signal electrode IDTs, ground electrode IDTs, reflectors, or a combination of these for local tuning of the piezoelectric coupling, to program the resonator frequency and S_{11} reflection coefficient as shown in Figure 1B. 200 nm ScAlN films with 22% and 30% doping were deposited on continuous Pt and Mo bottom electrodes respectively by reactive co-sputtering (Sc) of scandium and aluminum (Al) in nitrogen at an external vendor. A double-layer lift-off process was used to evaporate 10 nm/100 nm Ti/Au metal electrodes in the odd-hour evaporator.

The contact pads, routing lines, and test capacitors were patterned using SÜSS MA-6 contact photolithography (smallest features = 3 µm), and the metal IDTs were patterned using JEOL 6300 electron-beam lithography. The IDT widths were designed to 1 µm-400 nm, corresponding SAW frequencies in the 1-3 GHz range.

Figure 2 shows a Zeiss scanning electron microscope (SEM) image and zoom-in of a ScAlN SAW device with 400 nm IDTs including a process simulation to verify high-fidelity contact with the 2-layer evaporation.

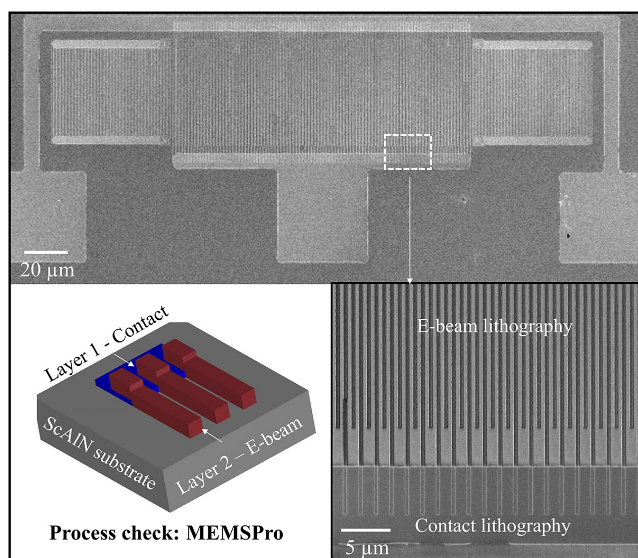

Figure 2: SEM image of a SAW device with 400 nm IDTs, including a zoom-in view of the overlapping metal layers patterned with e-beam and contact lithography. A 3D isometric view serves as a process check to confirm high-fidelity contact between the two layers.

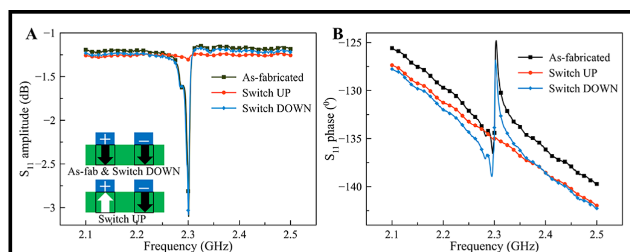

Figure 3: A) S11 amplitude (in dB) and B) phase (in 0) for a 2.3 GH 22% ScAlN SAW resonator showing two-state ScAlN programming. The as-fabricated, up-switched, and down-switched responses demonstrate reversible polarization switching, which enables turning off of the piezoelectric coupling and its full recovery to demonstrate a programmable resonator.

Results:

A setup with continuous wave positive-up-negative-down (PUND) was used for ferroelectric testing of $Sc_xAl_{1-x}N$ [2]. Single-sided triangular pulses of ± 6 MV/cm (larger than the coercive field), were applied to the SAW signal IDTs to sequentially up-switch and down-switch the ScAlN underneath them, followed by S_{11} measurements. Figure 3 shows S11 amplitude and phase responses of a 2.3 GHz 22% ScAlN SAW device for as-fabricated, up-switched and down-switched (±6MV/cm) pulses. The resonance vanishes with up-switching of ScAlN due to an ensemble switching off of the piezoelectricity, but can be fully recovered with down-switching. This process is repeatable over multiple cycles, demonstrating reversible switching of the resonator with minimal ScAlN degradation. The results show a pathway towards a CMOS-compatible filter with programmable frequency and amplitude control.

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Si-SiO_2 Metamaterial Ultrasonic Lens for Fourier Ultrasonics

CNF Project Number: 1121-03

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Primary CNF Tools Used: ASML DUV Wafer Stepper, Oxford 81 Etcher, Unaxis 770 Deep Silicon Etcher, Plasma-Therm Deep Silicon Etcher, Thermal Oxidation Furnace

Abstract:

Modern signal processing and machine learning greatly depend on high-performance and power-efficient computation. Fourier transform is one of the most widely used mathematical algorithms in signal processing, speech recognition, and image processing. The complexity of the digital fast Fourier transforms scale in the order of O(N^2logN), requiring significant computational resources for large data sets. It has been shown that ultrasonic waves can compute the Fourier transform with a planar lens at the focal length of the input. In this research, we fabricated a planar metamaterial lens that can bend the ultrasonic waves to form the Fourier transform at the lens's focal length.

Summary of Research:

The Fourier transform is a mathematical formula that transforms its time component into the frequency domain. Fourier transform is one of the most widely used algorithms with applications in signal processing, machine learning, and finance. Additionally, the computation power and efficiency of Fourier transform are needed to meet the exponential growth of data in both industries and science. Modern computation frameworks rely on transistor-based processing units. However, it became challenging to continue Moore's law and meet the need for power-efficient computation as the size of the transistor reduced. The Fourier transform using the ultrasonic wave is an alternative solution that can drastically reduce the computation time and power consumption [1-5].

The propagation of waves can be calculated by the Huygens-Fresnel principle. The Huygens-Fresnel principle could be computed from the Rayleigh-Sommerfeld diffraction formula and further simplified for the far-field as the Fraunhofer approximation. However, the Fraunhofer approximation contains an additional quadratic compared to the exact 2D Fourier transform.

In this work, we present a Fourier transform accelerator using the properties of waves. In order to obtain the exact Fourier transform at the receiver side, the accelerator requires a planar lens in front of the transmitter.

Numerous planar binary Fresnel lenses were presented in the past. They consist of binary phase shifts represented by the 2-step size of the lens. In this work, we present a metamaterial lens by fabricating a 4-step size lens and changing the fraction between silicon and SiO_2. This fabrication process only requires a single mask and yields a higher diffraction efficiency which is the ratio between the energy at the focal point and the incoming wave [1-3].

The lens is fabricated by establishing spatially varying SiO_2 pillars inside the silicon wafers that correspond to the different indices of refraction to the passing waves, as shown in Figure 1. The mask is analytically calculated and designed with python to generate the final GDS file. ASML DUV stepper is used for photolithography with pillar diameter of 500 nm - 1 µm. The silicon wafer is etched 16 µm with deep reactive ion etching (DRIE), as shown in Figure 1. SEM pictures are taken after the DRIE

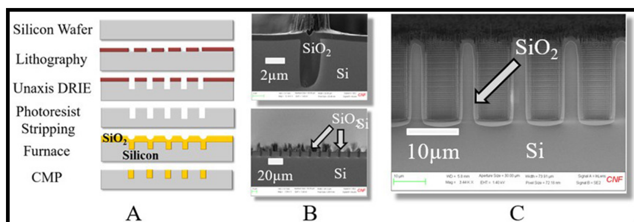

Figure 1: The process flow and SEM pictures after oxidation. A. is the process flow of the ultrasonic lens. B. and C. are the SEM picture after the wet furnace oxidation. The device SEM pictures show the filled trenches of SiO_2 on the silicon wafer [3].

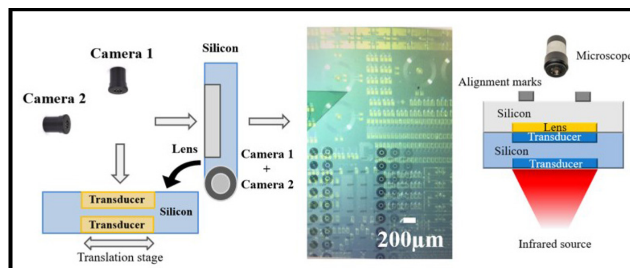

Figure 3: The final lens is bonded to the AlN transmitter using the Pico MA fine-placer. The flip-chip bonder shows the two devices on the same screen overlapping each other [3].

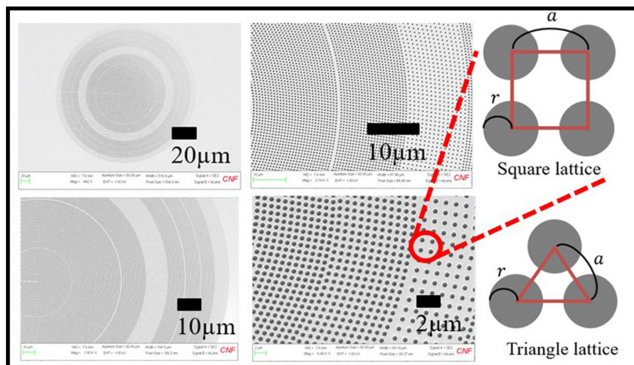

Figure 2: The top-side SEM images of the final device. The varying spatial distribution of the pillar corresponds to a different index of refraction for the acoustic waves. The size of the lens varies from 100 µm to 200 µm in diameter [3].

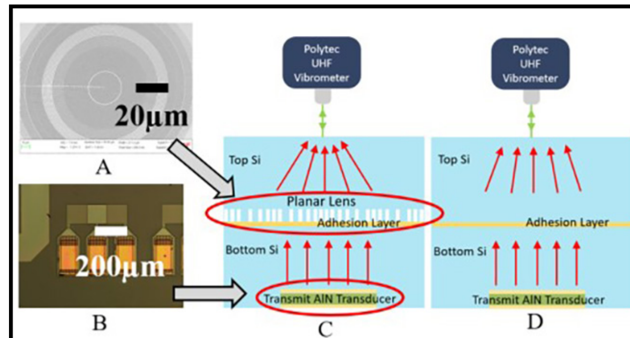

Figure 4: After bonding the lens with the AlN transmitter, the focusing effect is tested with the Polytec UHF [3].

to verify the exact etching rate of the DRIE. Then the trenches are filled with oxide by wet thermal oxidation at 1100°C for 100 minutes. Finally, the device is flattened by chemical mechanical polishing (CMP) and diced using the DISCO.

The final planar metamaterial lens is shown in Figure 2, where the different radii of the pillar spacing represent the different indices of refraction [2].

The final device consists of lenses with a focal length of 500 µm and 1 mm at 1.2 GHz, as shown in Figure 2. After the final fabrication, the device is bonded to the double-sided square transducer actuators fabricated from IME-ASTAR Foundry as shown in Figure 3. The flip chip bonder is used to align the lens and the AlN transmitter for the bonding. Additionally, the infrared microscope was used to verify the alignment after bonding. Finally, the bonded device was tested under Laser Doppler Vibrometry (LDV) to measure the lens's focusing power, as shown in Figure 4 [3].

Conclusions and Future Steps:

In this work, we presented a planar GHz lens that can focus the ultrasonic waves generated from a 100 µm × 100 µm AlN transducer. The lens consists of spatially varying SiO_2 pillars embedded in the silicon wafer to induce different indices of refraction for the incoming waves. The final device was tested using the Polytec UHF to show the focusing effect of the lens at 676 MHz and 1.016 GHz. The demonstrated lens is a preliminary result of the metamaterial lens necessary to make the Fourier transform accelerator.

References:

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HZO-Based Ferro NEMS MAC for In-Memory Computing

CNF Project Number: 1121-03

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Primary CNF Tools Used: SÜSS MA-6 Contact Aligner, CVC SC-4500 Odd-Hour Evaporator, Zeiss SEM, OEM Endeavor M1, Plasma-Therm Takachi HDP-CVD, Arradiance ALD, AJA Sputter Deposition, Oxford PECVD, Oxford 81/82, Primaxx Vapour HF Etcher, UN770 Etcher, YES EcoClean Asher, Xactix Xenon Difluoride Etcher, AJA Ion Mill, Heidelberg Mask Writer-DWL2000, P7 Profilometer, Zygo Optical Profilometer, Flexus Film Stress Measurement

Abstract:

This work details the fabrication of a hafnium zirconium oxide (HZO)-based ferroelectric NEMS beam as the fundamental building block for very low-energy capacitive readout in-memory computing. The demonstration device consists of a 250 × 30 µm unimorph cantilever of 20 nm thick ferroelectric HZO on 1 µm SiO_2. The displacement of the piezoelectric unimorph was measured by actuating the device with different input voltages V_{in}. The resulting displacement was measured as a function of the ferroelectric programming voltage V_p. The beam displacement scale factor was measured to be 182.9 nm/V for -8V V_p and -90.5 nm/V for 8V V_p, demonstrating that the programming voltage can be used to change the direction of motion of the beam. The resultant output beam displacement from AC actuation is in the range of -15 to 18 nm and is a scaled product of the input voltage and programmed d_{31} (governed by the poling voltage). The multiplication function serves as the fundamental unit of MAC operations with the ferroelectric NEMS beam.

Summary of Research:

Neuromorphic computation is of great interest to computing theory and practical implementations due to the potential for low-power, high efficiency, and small form factor information processing with deep neural networks (DNN) [1,2]. With the ever-increasing number of variables required for neuromorphic computation with high accuracy, there is an urgent need to develop highly energy-efficient device architectures [2-4]. FET-based in-memory computation architectures are susceptible to large read and write energy consumption and high leakage currents in idle mode, particularly with gate dielectric thickness scaling down to < 5 nm [5]. NEMS switches and beams offer an alternate pathway to zero-leakage in-memory compute synaptic functionality, provided that the beam actuation has embedded programmable weights in the form of tunable capacitive or piezoelectric coupling.

While analog in-memory computing has been demonstrated using different architectures that use transistors or memristors, few prior works have used a

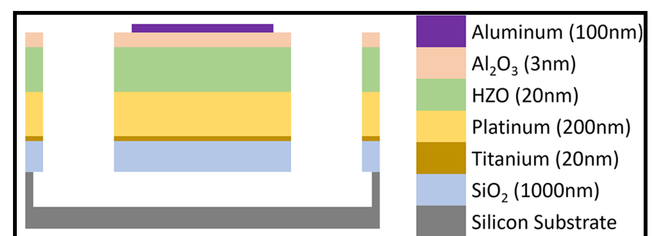

Figure 1: Schematic cross-section view of the ferroelectric beam.

NEMS-based approach that takes advantage of released beam structure to eliminate energy leakage in an idle state [6].

In this work, we present a ferroelectric/piezoelectric beam transducer to enable the multiplication that can be read out capacitively eliminating any DC currents.

Figure 1 shows the cross-section view of the clamped-clamped unimorph ferroelectric beam used to

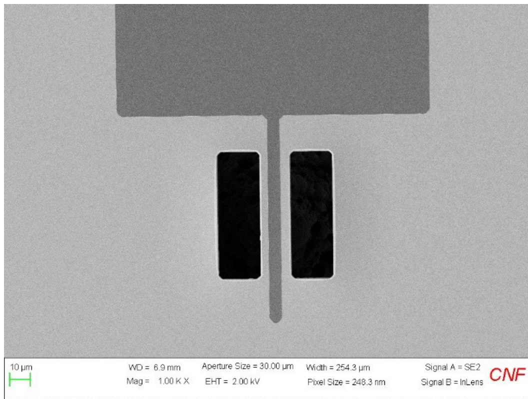

Figure 2: SEM of the beam showing the released structure.

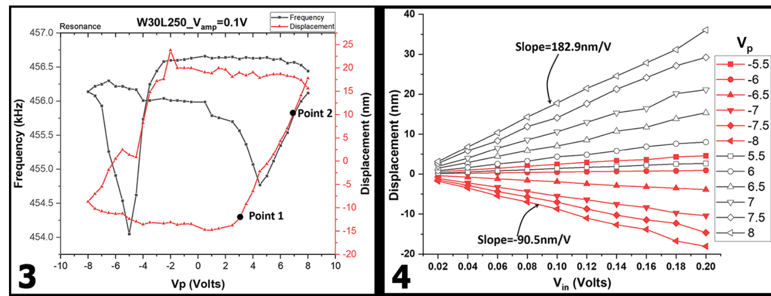

Figure 3, left: Central beam displacement δ_{max} and resonant frequency f_0 vs. poling voltage V_p. Figure 4, right: The displacement vs. V_{in} for different values of the V_p.

demonstrate piezoelectric coefficient programming. 1 µm thick thermal SiO_2 forms the passive elastic layer underneath the 20 nm ferroelectric HZO. The HZO is capped by 3 nm of alumina (Al_2O_3), followed by annealing at 400°C to crystallize the HZO in its ferroelectric orthorhombic phase. Then 200 nm platinum (Pt sputtering) and 100 nm Al (Al evaporation) were deposited to form the bottom and top metal electrode contacts for the HZO respectively. Pt was etched using AJA ion mill and the liftoff technique was used to pattern the Al electrode. The beam was released by isotropic etching of the silicon substrate using Xactix XeF_2.

A Zeiss scanning electron microscope image of the fabricated device is shown in Figure 2.

After release, the beams were observed to be buckled due to residual film stress generated during microfabrication. A 3D optical profilometer (Zygo™ system) was used to measure the beam buckling profile. The maximum displacement for a 250 × 30 µm was 4.98 µm.

Figure 3 shows the central beam displacement δ_{max} and resonant frequency f_0 vs. poling voltage V_p plot in the frequency range of 450 to 460 kHz for the nominal 250 × 30 µm ferroelectric clamped-clamped beam presented here. Peak displacement δ_{max} (red line) is modulated for different values of V_p and traces a hysteresis loop. The net effect of the number of upward and downward pointing dipoles that control the macroscopic polarization in the beam (induced due to V_p) also changes the beam stiffness resulting in resonance frequency modulation (black line), which presents a separate modality of memory storage in the beam. The two dips in f_0 correspond to the positive and negative coercive fields of the HZO film where the net polarization is almost zero.

To show the effect of V_{in} on δ_{max}, we swept V_{in} from 0.02V to 0.20V for different values of the V_p. Figure 4 shows a plot of δ_{max} vs. V_{in} at different values of V_p, which emulates the transfer characteristics of the analog multiplier. For constant poling voltages, if we sweep the inputs, we get a linear increase in displacement value. Similarly, for constant inputs, different poling voltages outputs different displacement values.

In conclusion, we have demonstrated an HZO-based NEMS multiplier weight storage functionality. The device was fabricated and characterized, showing the dependence of beam displacement on the poling voltage of the ferroelectric film. The frequency tunability was also demonstrated that can be further explored to realize unique features such as an electrically tunable filter. Future work will build on this demonstration for device scaling towards high device density.

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HF Vapor Release Etch

CNF Project Number: 1611-07
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Affiliation(s): Department of Electrical Engineering University of Notre Dame

Primary Source(s) of Research Funding: National Science Foundation
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Primary CNF Tools Used: Primaxx Vapor HF Etcher

Abstract:

Reversible computing reduces the energy dissipation of a circuit by using logical reversibility and quasi-adiabatic transitions, introducing a trade-off between energy and speed. Adiabatic CMOS is the most developed implementation of reversible computing, but it is ultimately limited by passive power, the energy dissipation caused by leakage. New computing approaches try to eliminate the leakage current completely by using micro-electro-mechanical systems (MEMs) as relays to implement computing. Unlike CMOS circuits, the MEMs relays do not have a subthreshold current since they have no electrical contact when they are off. However, the relays will wear out over time primarily due to degradation of the current-carrying contacts. Adiabatic Capacitive Logic (ACL) was proposed by Pillonnet and Houri as a novel approach to reversible computing that eliminates leakage current and does not have make and break contacts therefore avoiding the degradation problem seen in relays. The fabrication of these nano-relays requires a release etch to free the MEMs structures. A wet etch process with critical-point drying gave a very low yield, so a vapor HF process at the Cornell NanoScale Facility (CNF) was used instead.

Summary of Research:

The basic structure is shown in the diagram of Figure 1 in cross section. A control voltage is applied between the plates on the left side which pulls down the upper plate, changing the capacitance of the output capacitor at the right. A key step in the process is a vapor hydrofluoric acid (HF) release etch, performed at CNF using the Primaxx Vapor HF Etcher, instead of the liquid HF followed by critical point drying that we used previously. This greatly increased the yield of process, since the critical point dryer was a very difficult process to control, and nearly all devices would stick to the surface during the drying process. With the vapor process the yield increased to about 50% in the first two runs. One disadvantage of the vapor HF process is that the vapor etches the TiN electrode layer more than in a liquid HF process. This resulted in an increased access resistance between the probe pads and the device that adversely impacted the capacitance measurements.

An SEM micrograph of the finished device is shown in Figure 2. There is still some residual stress in the polysilicon layer that causes the springs to bend out of plane. During the fabrication the samples are given a high-temperature treatment after the polysilicon deposition that is intended to relieve stress in the film, but this process needs further optimization. Initial measurements show that the devices operate correctly, and the characteristics of the devices are being measured. A pull-in voltage at an average of 22V is observed, in close agreement with COMSOL simulations.

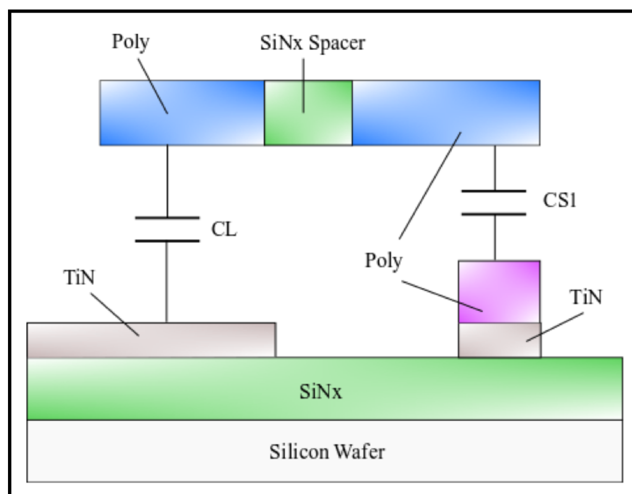

Figure 1: Voltage-controlled variable capacitor gap closing structure.

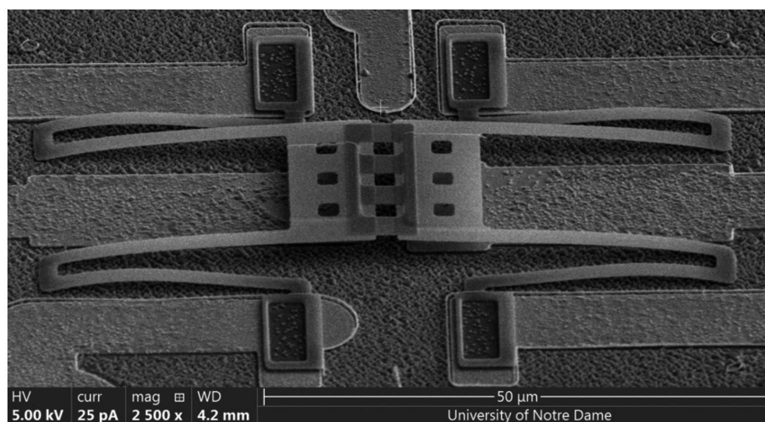

Figure 2: SEM micrograph of completed ACL variable capacitor.

ELECTRONICS

MBE Grown AlScN/AlN/GaN High Electron Mobility Transistors with Regrown Contacts

CNF Project Number: 2438-16

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Primary CNF Tools Used: Autostep i-line Stepper, Heidelberg Mask Writer - DWL2000, P7 Profilometer, FilMetrics, AFM Veeco Icon, Zeiss SEM, PT 770, Oxford 81, Oxford ALD / PECVD, SC4500 Evaporators, AJA Sputter Deposition, RTA AG610, JEOL 9500

Abstract:

We report the first observation of ferroelectric gating in AlScN barrier wide-bandgap nitride transistors. These FerroHEMT devices realized by direct epitaxial growth represent a new class of ferroelectric transistors in which the semiconductor is itself polar, and the crystalline ferroelectric barrier is lattice-matched to the substrate. The FerroHEMTs reported here use the thinnest nitride high-K and ferroelectric barriers to date to deliver a high on-currents at 1.34 A/mm, and highest speed AlScN transistors with f_{MAX} > 150 GHz observed in any ferroelectric transistor. The FerroHEMTs exhibit hysteretic I_d-V_{gs} loops with subthreshold slopes below the Boltzmann limit. A control AlN barrier HEMT exhibits neither hysteretic nor sub-Boltzmann behavior. While these results introduce the first epitaxial high-K and ferroelectric barrier technology to RF and mm-wave electronics, they are also of interest as a new material platform for combining memory and logic functionalities in digital electronics.

Summary of Research:

The GaN/$Al_{0.86}Sc_{0.14}N$/AlN/GaN HEMT structure consists of a 2 nm GaN cap layer, a 5 nm $Al_{0.86}Sc_{0.14}N$ barrier, a 2 nm AlN spacer (total barrier thickness: 9 nm), a 1000 nm unintentionally doped GaN channel, and AlN nucleation layer on a SiC substrate, grown by plasma assisted molecular beam epitaxy (PA-MBE). Room temperature Hall-effect measurements with In-dots prior to device fabrication showed a 2DEG sheet concentration of 2.99 × 10^{13}/cm^2 and electron mobility of 500 cm^2/V·s, corresponding to a sheet resistance of 417 Ω/sq.

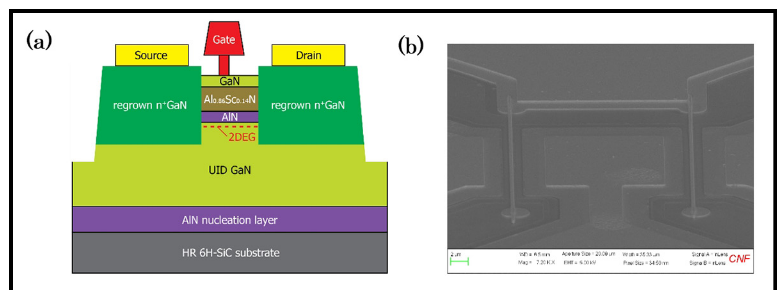

Figure 1: (a) Schematic cross-section and (b) SEM image of AlScN/AlN/GaN HEMTs on 6H-SiC with regrown n^+GaN contacts.

A schematic cross-section of the AlScN/AlN/GaN HEMT device with regrown n^+ GaN contacts is shown in Figure 1(a). The device fabrication process started with patterning of a SiO_2/Cr mask for n^+GaN ohmic regrowth by PA-MBE. The pre-regrowth etch depth into the HEMT structure was 40 nm, and regrown n^+GaN was 100 nm with a Si doping level of 7 × 10^{19}/cm^3. Non-alloyed ohmic contact of Ti/Au was deposited by e-beam evaporation. T-shaped Ni/Au (30/350 nm) gates were formed by e-beam lithography, followed by liftoff. TLM measurements yielded a contact resistance of 0.31 Ω·mm.

The device presented here has a regrown n^+GaN source-drain distance L_{SD} of 600 nm, a gate width of 2 × 25 µm, and a gate length L_G of 90 nm. An SEM image of completed AlScN/AlN/GaN HEMT is shown in Figure 1(b).

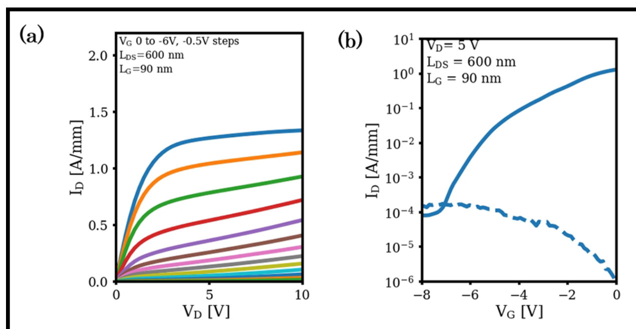

Figure 2: (a) Family I-V curves and (b) transfer characteristics of the device with L_G = 90 nm and L_{SD} = 600 nm.

Figure 2(a) shows the family I-V curves of the device, measured for V_{DS} = 0 to 10 V and V_{GS} = 0 to -6 V. The device has a saturation drain current I_{DSS} = 1.34 A/mm and an on-resistance R_{ON} = 1.4 Ω·mm extracted at V_{gs} = 1 V. The transfer curves are shown in Figure 2(b). A peak extrinsic transconductance g_m is 0.46 S/mm at V_{DS} = 5 V.

Figure 3(a) shows the current gain $|h_{21}|^2$ and unilateral gain U of the device as a function of frequency at the peak f_T bias condition, V_{DS} = 10 V, and V_{GS} = -1.4 V.

The extrapolation of both $|h_{21}|^2$ and U with -20 dB/dec slope gives the current gain cutoff frequency/maximum oscillation frequency f_T / f_{MAX} of 78/156 GHz after de-embedding. The f_T and f_{MAX} of the device are summarized in Figure 3(b), showing how the results of this device compare with the early state-of-art results of AlScN/GaN HEMTs on SiC substrates [1-3].

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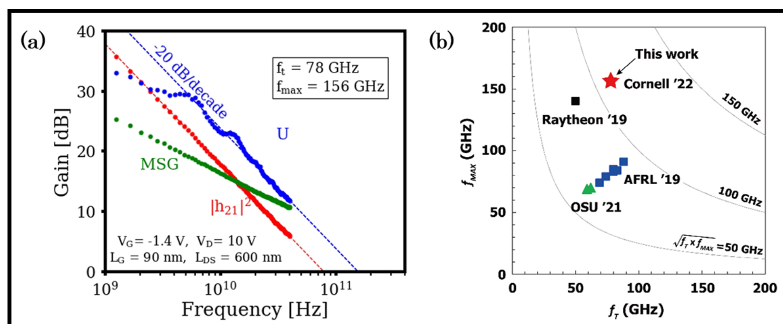

Figure 3: (a) Current gain and unilateral gain of the device with L_g = 90 nm, showing f_T / f_{MAX} = 78/156 GHz. (b) Comparison of the measured f_T and f_{MAX} of $Al_xSc_{1-X}N$/GaN HEMTs.

Fabrication and Manipulation of Micro-Scale Opto-Electrically Transduced Electrodes (MOTEs)

CNF Project Number: 2658-18 & 2836-19

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Primary CNF Tools Used: ABM Contact Aligner, AJA Sputter, Westbond 7400A Ultrasonic Wire Bonder, Oxford 81/82/100, Unaxis Deep Si Etcher, Oxford PECVD, Oxford ALD, Anatech, P7 Profilometer, Zeiss Ultra and Supra Scanning Electron Microscopes

Abstract:

Recording neural activity in live animals *in vivo* is critical in elucidating how the brain functions. However, such recording poses several challenges. Electrical techniques typically require electrodes to be tethered to the outside world directly via a wire, or indirectly via an RF coil [1], which is much larger than the electrodes themselves. Tethered implants suffer from the residual motions between electrodes and neurons as the brain moves, limiting our ability to measure from peripheral nerves in moving animals, especially in smaller organisms such as zebra fish or fruit flies. On the other hand, optical techniques, which are becoming increasingly potent, are often limited to subsets of neurons in any given organism, impeded by scattering of the excitation light and emitted fluorescence, and limited to low temporal resolution [2]. Here we present an untethered opto-electrical system on chip (SoC), Micro-scale Opto-electrically Transduced Electrodes (MOTEs), which are powered by, and communicating through, a microscale optical interface, combining many benefits of optical techniques with high temporal-resolution of electrical recording.

Summary of Research:

Our fabrication starts with about 5 mm × 5 mm, conventional 180 nm CMOS die, which contains the electronics for signal amplification, encoding, and transmission. The CMOS die is then integrated with AlGaAs diode, which acts as a photovoltaic (PV) as well as light emitting diode (LED), hence the diode is abbreviated as PVLED. The PVLED provides an optical link which powers the electronics and transmits encoded signals in optical pulses. The MOTE utilizes Pulse Position Modulation (PPM) for signal encoding for its high information-per-photon efficiency, where the spacing between the output pulses is proportional to the measured electric field of neuronal signals across the measurement electrodes. Figure 1 depicts a conceptual deployment and system description of such MOTE [3].

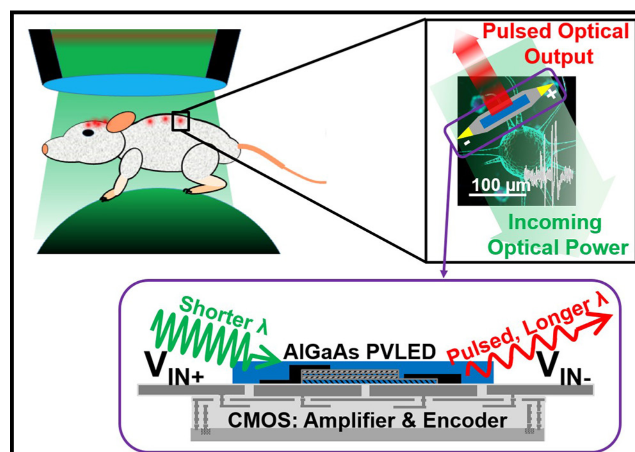

Figure 1: An exemplary implementation and system level description of the MOTEs in a mouse animal model [3].

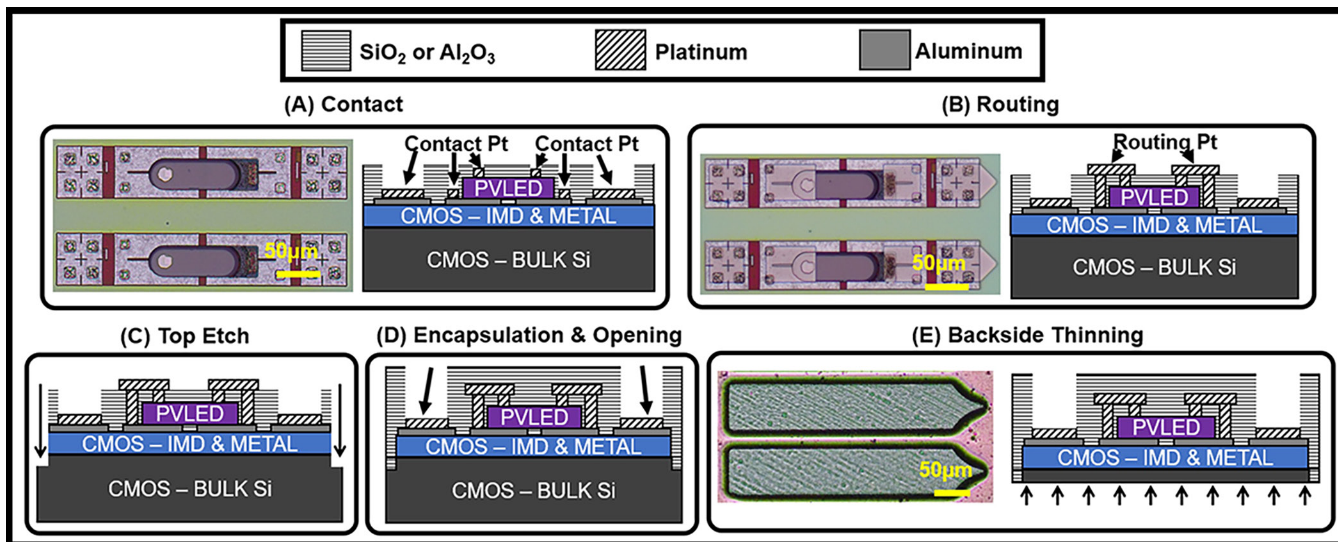

Figure 2: MOTE Fabrication Process. (A) An AlGaAs µLED (bullet-shaped) array is transferred on top of a CMOS chip containing an array of unit MOTE circuitry, and Pt is deposited over contact areas. (B) Routing Pt electrically connects each µLED with an underlying CMOS. (C) Each MOTE is segregated and (D) encapsulated with SiO_2 and Al_2O_3 except for the measurement electrodes area. (E) The backside Si is thinned so that total thickness is < 30 µm. Adapted from [4].

The AlGaAs diodes are first fabricated on a sapphire wafer, to be later released from the sapphire substrate with a sacrificial poly(methyl methacrylate) (PMMA) polymer. Once the PMMA-coated AlGaAs diodes are transferred onto the CMOS die, Oxford 81 plasma etcher is used to remove the sacrificial PMMA, leaving only the diodes array intact on the CMOS die. To establish the electrical contact between the PVLED and CMOS, we have used the CNF ABM Contact Aligner for photolithography with AZ nLof2020 UV photoresist for efficient lift-off process that ensues after metal deposition. After the contact fabrication, the contacts of CMOS and PVLED are connected via similar photo-lithography process, and to maximize the conformality of the metal routing, we employ AJA Sputter. Following the routing step, each MOTE is encapsulated using Oxford ALD and PECVD for SiO_2 and Si_3N_4 deposition, followed by dielectric etching using Oxford 100 and Unaxis deep reactive ion etch (DRIE) for release. Figure 2 described the fabrication sequence described herein.

It should be noted that before embarking on the nano/ micro-fabrication flow, to confirm the functionality of each module (CMOS and the diode), we use Westbond 7400A Ultrasonic Wire Bonder for board-level test. ZEISS ultra and supra scanning electron microscopes (SEMs) are also used to inspect the fabricated MOTE for debugging purposes.

Conclusions and Future Steps:

MOTEs are the smallest electrophysiological sensor of its kind, and we are currently testing the MOTEs *in vivo* in mouse animal models. As we accumulate more data on our ongoing *in vivo* efforts, we plan to improve fabrication processes as well as surgical procedures for inserting the MOTEs into the mouse cortex. Moreover, we are aiming to design MOTEs for electrochemical applications.

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High Frequency Sensors and Actuators for Ultrasonic Imaging

CNF Project Number: 2876-20

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Primary Source(s) of Research Funding: DARPA, ARPA-E, DOE
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Website: www.geegah.com
Primary CNF Tools Used: SÜSS MA6 Contact Aligner, PT740 Reactive Ion Etcher, E-Beam Evaporators, PECVD Deposition Tools

Abstract:

Geegah develops CMOS compatible ultrasonic imaging for fast and high-resolution environmental sensing; thanks to the high excitation frequencies (>1GHz) and lack of mechanical scanners that are typical to many commercial scanning acoustic microscopes. Using ultrasonic transducers made from aluminum nitride (AlN) deposited on top of CMOS, Geegah demonstrated imaging worms in soil, drying blood droplets, 3-D printed ink, fingerprints, and bacteria colony growth at frame rates more than 6Hz with 128 × 128 pixel arrays [1-3]. While the imaging chips are manufactured in a commercial CMOS foundry, early packaging of these systems were done in CNF.

For some applications that require imaging of soft materials or sensing over long distances in liquid, high acoustic impedance of AlN and large acoustic absorption due to high frequency of operation are not desired. To be used in this complementary set of applications, Geegah has been developing PVDF-TrFE spin-on piezoelectric films in CNF. These transducers are expected to operate at frequencies from 20 MHz to 600 MHz and are being fabricated using a three-mask process.

Summary of Research:

Planar ultrasonic transducers realized on silicon substrate emit ultrasonic waves through the piezoelectric effect. Amplitudes and nature of these waves are a function of the elastic properties of the transducer stackup as well as the frequency and amplitude of excitation. These ultrasonic waves can be used for imaging and sensing through pulse-echo operation where one transducer transmits and the other or the same transducer receives. Time-of-flight and amplitude of the received pulse in this process is used for sensing or imaging. Crystalline nature of the silicon substrate helps by providing a low acoustic loss medium as these waves propagate through the substrate.

The PVDF-TrFE is a much softer material than both silicon and AlN, and hence it is commonly used in biomedical sensing applications. Figure 1 shows the 3-mask process we developed to fabricate PVDF-TrFE transducers. The process starts with PECVD SiO_2 deposition on blank silicon wafer to serve as an insulation material. Then bottom electrode material, aluminum, is evaporated and patterned using the first mask and wet etching. Next, off-the shelf PVDF-TrFE powder is dissolved in a solvent and spun on the wafer to get thicknesses varying from 1.5 to 2.5 µm. The film thickness vs. spin-speed characterization curve is given in Figure 2. Following vacuum annealing and curing, the piezoelectric film is patterned using the second mask and an oxygen plasma etcher. Due to the reaction of standard photoresist removal solutions with the PVDF-TrFE film, a double exposure photoresist strip step is followed. Finally, a top metal layer is evaporated and patterned using the last mask.

Figure 3 shows the picture of a 200 µm diameter transducer after the lithography for the top electrode. Next steps involve dicing As for the high frequency imaging applications, Figure 4 illustrates a typical ultrasonic image acquired using Geegah's imaging chip, which was wirebonded and packaged in CNF. Here, the sample imaged is conductive ink printed directly on the surface of the imager for use in quality control of additive manufacturing [4].

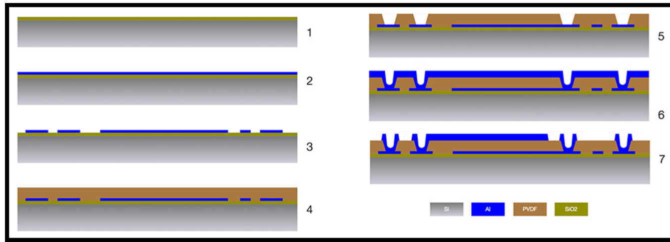

Figure 1: Process flow for the PVDF-TrFE ultrasonic transducer fabrication.

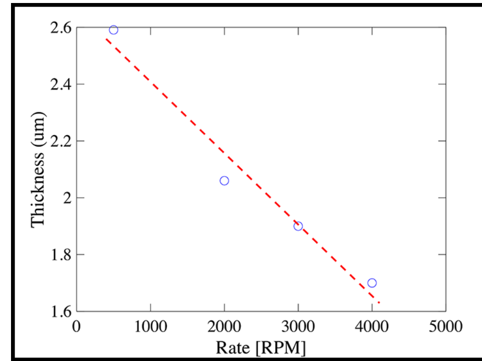

Figure 2: Characterization of the PVDF-TrFE thickness control using the spin-speed.

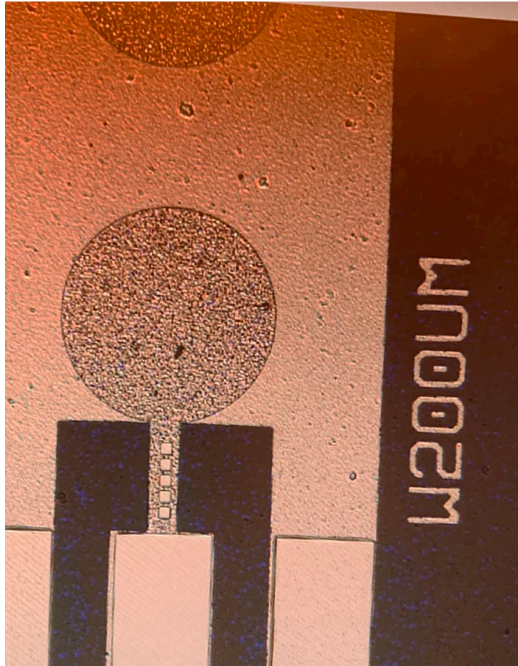

Figure 3: Picture of a fabricated 200 µm diameter device.

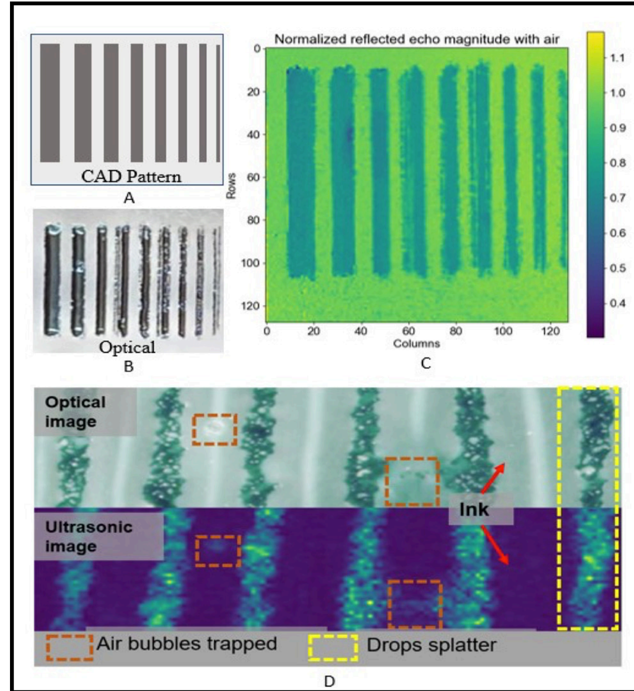

Figure 4: A) CAD pattern (grey area shows ink) for printed conductive ink lines. B) Optical image of the printed conductive ink on the imager surface. C) Ultrasonic image of the same ink patterns. D) Optical and ultrasonic images showing defects in the ink print pattern: air bubbles trapped within ink and tiny drops splattering between the ink lines [4].

In addition to imaging elastic properties, our results showed that the phase of the received echo carries signature of the temperature changes in the medium and sample.

Conclusions and Future Steps:

A PVDF-TrFE ultrasonic transducer is being developed to enhance imaging for materials with lower acoustic impedances or through longer fluidic coupling mediums. The three-mask process flow is close to completion and devices will be ready for testing following dicing and polarization. This process is expected to complement the high-frequency ultrasonic imaging capabilities and work with softer materials at lower excitation frequencies.

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General Electric Global Research Microfabrication Highlights 2022

CNF Project Number: 2993-21

Principal Investigator(s): Robert MacDonald

User(s): Robert MacDonald, Charles Szymanski, Timothy VandenBriel

Affiliation(s): General Electric Global Research
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Website: https://www.ge.com/research/electronics-sensing
Primary CNF Tools Used: SÜSS Bonder/Aligner, STPS uEtch HF Vapor Release, Schott IR Inspection Microscope

ELECTRONICS

Abstract:

Developments in analog computing have led to an interest in mechanical computing elements. We are persuing research in this field using small resonators and switches built in silicon.

Summary of Research:

We are developing analog computing elements out of mechanical structures. The structures are fabricated in silicon, so called 'NEMS', or nano electromechanical systems. The structures consist of resonant elements where computation is mapped to phase, frequency or amplitude. We fabricated these structures at our facility in Niskayuna, New York. We use the CNF as a backup for certain tools. In addition, we plan on using CNF to extend our capabilities to build smaller structures than we are capable of building in our own facility. We have not yet published our results in this area, with publications expected in 2023.

Our work is based on our GE 'Polaris' process, a foundry process which we offer commercially. Polaris has been used to fabricate accelerometers and gyroscopes, with future projects slated for timing, pressure and strain sensing.

Conclusions and Future Steps:

We expect to publish results in 2023 on our mechanical computing devices, when we will have more data to report.