Test Chip for Impedance Spectroscopy of Neuro Excitability

CNF Project Number: 2832-19

Principal Investigator(s): Prof. Huili Grace Xing

User(s): Mohammad Javad Asadi

Affiliation(s): School of Electrical and Computer Engineering, Cornell University

Primary Source(s) of Research Funding: Air Force Office of Scientific Research

Contact(s): grace.xing@cornell.edu, ma2297@cornell.edu

Primary CNF Tools Used: ABM contact aligner, SÜSS MA6-BA6 contact aligner, GCA AutoStep 200 DSW i-line wafer stepper, Heidelberg mask writer, Glen 1000 resist strip, CVC SC4500 odd-hour evaporator, Zeiss Supra SEM

Abstract:

This report focuses on the efforts for fabrication of a test chip containing coplanar waveguides and designed for impedance spectroscopy of neuron excitability. Since there has been a mysterious problem during the fabrication of the chip, we elaborate on the efforts to find the root cause of this issue. Finally, some conclusions will be provided along with suggestions to be tried to alleviate the problem.

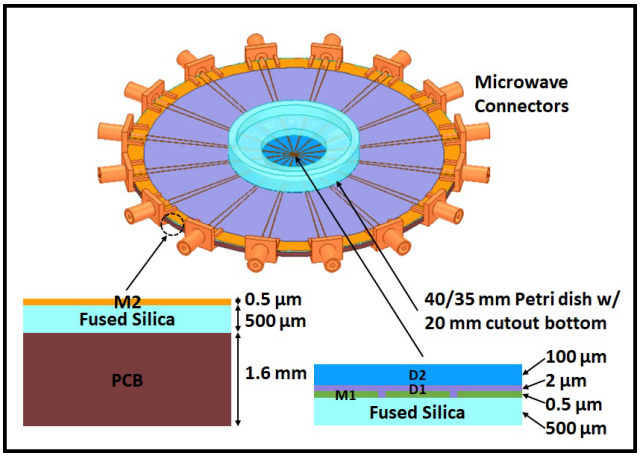

Figure 1: Top view of the designed test chip mated with a Petri® dish.

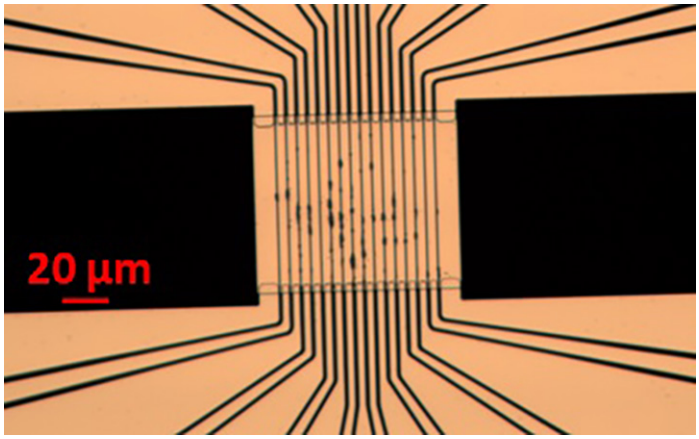

Figure 2: Micrograph of the gold M1 and M2 fabricated on a fused silica wafer.

Summary of Research:

Figure 1 shows the designed test chip. It can be seen that the chip serves as the bottom of a Petri® dish reservoir through a 20-mm-diameter cutout in the bottom of the Petri dish. The chip comprises eight coplanar waveguides (CPWs) fabricated on a 0.5-mm-thick, 100-mm-diameter fused silica wafer. Sixteen microwave connectors of sub-miniature type A (SMA) are attached on the edge of the fused silica wafer in a radial pattern. The fused silica wafer is mechanically strengthened by a 1.6-mm-thick FR4 printed circuit board (PCB) with a 40-mm cutout to allow transmission optical microscopy of the center portion of the fused silica wafer. A microfluidic channel (100 μm long, 20 μm wide, 2 μm high) for axons is formed on the fused silica wafer with 2-μm-thick SU-8 walls and a 100-μm-thick polydimethylsiloxane (PDMS) cover. To electrically insulate the CPWs from the culture medium outside the microfluidic channel, the SU-8 covers most of the fused silica wafer and the PDMS covers most the cutout of the bottom of the Petri dish.

The fabrication process for the entire chip is a four-mask process. The first two layers that were fabricated are metal 1 (M1) at the center of the chip, and metal 2 (M2) for the rest. The photolithography for M1 was done using the GCA AutoStep 200 DSW i-line wafer stepper to create a pattern with gaps of 1 μm. CVC SC4500 odd-hour evaporator was used to deposit 15 nm and 200 nm of titanium and gold, respectively, as M1. The same process but using SÜSS MA6-BA6 contact aligner was done to deposit 15 nm and 500 nm of titanium and gold respectively, as M2. The fabricated two metal layers is shown in Figure 2.

As can be seen in the figure, once M2 is deposited, and lift-off process is done, the M1 starts to develop some mouse bites. However, this kind of defects never observed in M1 before M2 is deposited and lifted off.

As a scanning electron microscopy (SEM) image of the M1, shown in Figure 3 confirms, the metal is severely damaged after fabrication. In order to solve this problem, several suggestions were tried such as not using RCA cleaning, not sonication for lift off, using brand new crucibles and metal sources for evaporation, and prebaking the wafers for several days before fabrication. However, none of these suggestions were helpful.

Successful fabrication without any mouse bite on a silicon wafer instead of fused silica led us to come up with a hypothesis that the problem is due to the electrostatic discharging effect.

In order to verify this hypothesis, half of the coplanar waveguide lines fabricated using aluminum were shorted while kept the rest intact. The result is shown in Figure 4.

As can be seen, the metal lines that are shorted and cannot build up static charge, are not damaged while the others developed mouse bite although not as severe as the case fabricated with gold. This test validates the assumption that the defects (mouse bites) are due to the electrostatic discharging that happens between each two isolated electrodes.

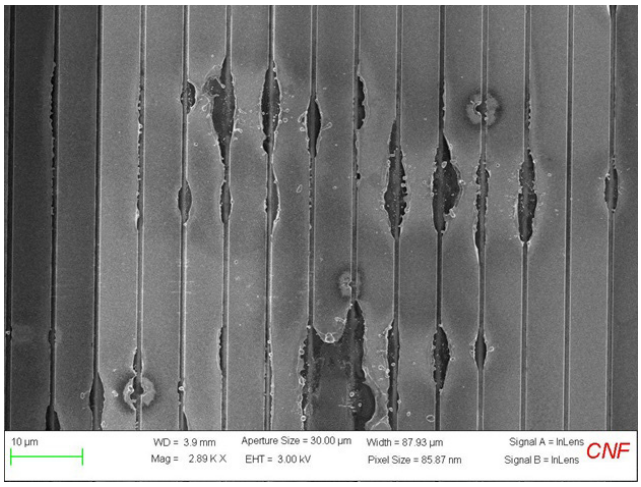

Figure 3: SEM image of the mouse bites in M1.

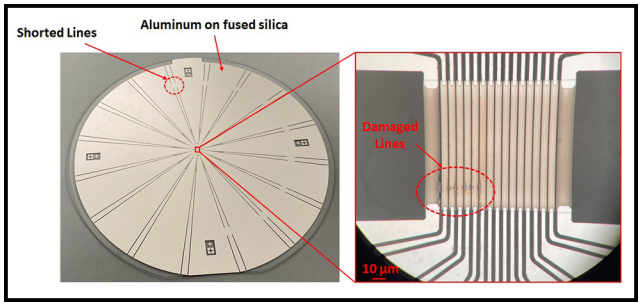

Figure 4: Micrograph of the aluminum M1 and M2 fabricated on fused silica wafer.

Conclusions and Future Steps:

We successfully found the root cause of the mouse bites that developed in the metal layer fabricated on a fused silica wafer. In the future, the isolated metal layers will be temporarily shorted up to the last fabrication step to make sure electrostatic discharging will not happen. Besides that, the fabricated metal layers will be covered with a thin layer of oxide that might help to mitigate the electrostatic discharging effect.