Charge-Order-Enhanced Capacitance in Semiconductor Moiré Superlattices

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Primary CNF Tools Used: Autostep i-line stepper, Hamatech wafer processor develop, Heidelberg mask writer - DWL2000, photolithography spinners, CVC SC4500 odd/even-hour evaporator, DISCO dicing saw

Abstract:

Van der Waals moiré materials have emerged as a highly controllable platform to study the electronic correlation phenomena. In particular, robust correlated insulating states have recently been discovered at both integer and fractional filling factors of the semiconductor moiré systems. In this project, we study the electronic compressibility of $MoSe_2/WS_2$ moiré superlattices by capacitance measurements. Our results reveal the thermodynamic properties and illustrate mechanism for enhanced capacitance in semiconductor moiré superlattices.

Summary of Research:

Quantum capacitance C_Q represents electronic compressibility or thermodynamic density of states of an electronic system that relates to its thermodynamic properties [1]. Quantitative measurement of C_Q can be realized by measuring differential capacitance per unit area C ($C^{-1} = C_g^{-1} + C_Q^{-1}$ with C_g denoting the geometrical capacitance between sample and gate) [2]. Semiconductor moiré superlattices host strongly correlated insulating states [3]. In this project, we demonstrate capacitance measurements on such system, which not only provide thermodynamic quantities but also offer new insight into correlations in van der Waals heterostructures.

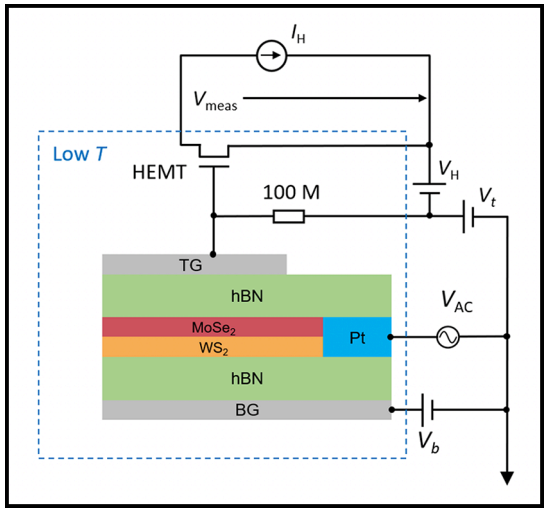

Figure 1: Schematics of a dual-gate device structure and electrical connections for capacitance measurements. TG and BG denote the top and back gate, respectively.

Figure 1 shows the schematics of dual-gated device structures and electrical connections for capacitance measurements. The device is made of an angle-aligned $MoSe_2$ and WS_2 heterobilayer encapsulated by top and bottom graphite gates separated by hexagonal boron nitride (h-BN) dielectrics. Angle-aligned $MoSe_2/WS_2$ heterobilayers form a triangular moiré superlattice with moiré period $a_M \approx 8$ nm due to 4% lattice mismatch between these materials. A commercial high electron mobility transistor (HEMT, model FHX35X) is used as the first-stage amplifier to effectively reduce the parasitic capacitance from cabling [4]. To obtain the top gate capacitance, we apply an AC voltage (10 mV in amplitude) to the moiré superlattice and collected the signal from the top gate through the HEMT.

Figure 2 is an optical image of a typical device. The Pt electrodes are patterned on the Si/SiO_2 substrates by photolithography and metal evaporation. Atomically thin samples of $MoSe_2$, WS_2, h-BN, and graphite are first exfoliated from their bulk crystals onto silicon substrates covered with a 300 nm thermal oxide layer. Selected thin flakes of appropriate thickness and geometry are then picked up one-by-one by a stamp consisting of a thin layer of polycarbonate on polydimethylsiloxane (PDMS). The complete heterostructure is then deposited onto the substrates with pre-patterned Pt electrodes.

Figure 3 shows the measured differential capacitance C in the unit of C_g as a function of top gate voltage measured at 10 K and bottom gate voltage V_b = 5.3 V. We observe a step increase of capacitance around -4 V when the Fermi level enters the conduction band of $MoSe_2$. The capacitance plateaus out above ~ 0 V when the sample is heavily electron doped. We calibrate capacitance using these two limits: $C / C_g = 0$ when the Fermi level lies inside the superlattice band gap (> 1 eV) and the sample is insulating (incompressible); $C / C_g \approx 1$ when the sample is heavily doped and behaves as a good conductor. At intermediate gate voltages, we identify a series of capacitance dips (incompressible states). The most prominent ones appear equally spaced in gate voltage and are assigned integer fillings ν = 1, 2, 3 and 4. The assignment is consistent with the known moiré density and the carrier density n evaluated from the gate voltage and $C_g \approx 2.1 \times 10^{-7}$ Fcm^{-2}. The latter is determined from the permittivity and thickness of the h-BN gate dielectric d ($\varepsilon \approx 3\varepsilon_0$ with ε_0 denoting the vacuum permittivity).

It was independently verified by including a reference capacitor on the measurement chip.

We observe anomalously large capacitance in the compressible regions between the incompressible states. The enhancement is particularly large at small doping densities with C exceeding C_g by ~ 30% for device with $d/a_M \approx 1$. Figure 4 shows devices of different sample-gate separation ($d/a_M \approx 0.6, 0.8, 1.0$ and 1.5). The capacitance enhancement increases with decreasing d/a_M. It is as high as 60% in device with $d/a_M \approx 0.6$ at 10 K.

The experimental results show that the correlation effects are strongly dependent on sample-gate separation in devices with $d/a_M \sim 1$, particularly, for the fractional-filling states since the gate electrodes effectively screen the extended Coulomb interactions. In this regime where electronic interactions dominant and sample gate distance is comparable to electron separations, we need to describe the entire device as one system [5].

In conclusion, our study establishes capacitance as a powerful thermodynamic probe of the correlated states in semiconductor moiré superlattices. It also illustrates the importance of sample-gate coupling and the device-geometry-dependent extended Coulomb interaction at fractional fillings.

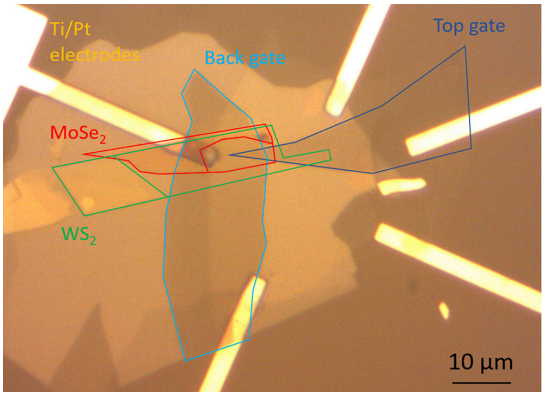

Figure 2: Optical microscope image of a dual-gate device. Colored lines show the boundary of the $MoSe_2$, WS_2, top gate and bottom gate flakes, respectively. Scale bar is 10 μm.

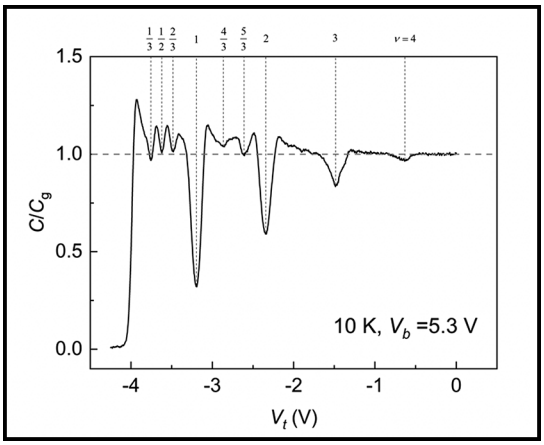

Figure 3: Differential top gate capacitance as a function of top gate voltage at 10 K for Device with $d/a_M \approx 1$. The back gate voltage is fixed at 5.3 V. The filling factors for discernable incompressible states are labeled on the top axis.

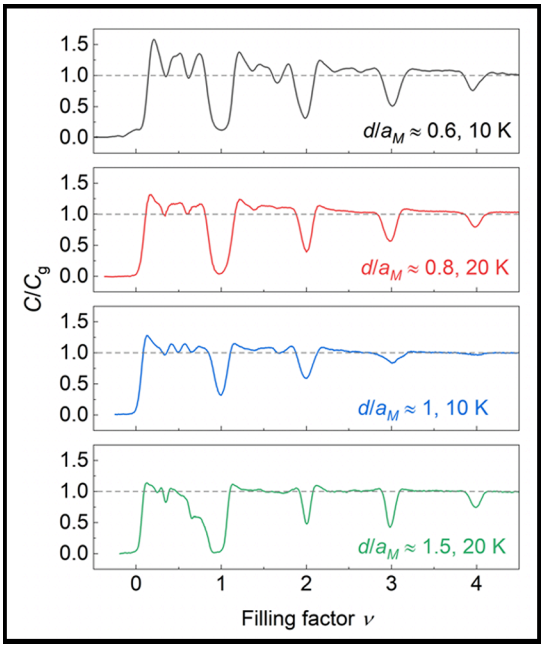

Figure 4: Experimental top gate capacitance as a function of filling factor for devices with $d/a_M \approx 0.6, 0.8, 1.0$ and 1.5 (from top to bottom) at the lowest temperature (10 K or 20 K) allowed by the sample/contact resistance.

References:

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