Inkjet-Printed Colloidal Quantum Dot Superlattices

Abstract:

In this work, we investigated whether inkjet printing is a suitable method to form nanocrystal superlattices on top of (sub-)mm sized droplets or not. We identified the choice of solvent as a bottleneck in the process. We reviewed and adapted the common and system-specific constraints and found a suitable candidate. We successfully prepared highly ordered superlattices using dodecane, and explored the limitations of the approach.

Summary of Research:

Colloidal quantum dot (CQD) superlattices with epitaxial connections between the constituents are exciting bottom-up fabricated metamaterials with properties adjustable between zero and three dimensions. Assemblies can be achieved on solid substrates, but the shrinkage and consequent mechanical strain following the fabrication leads to cracks and low domain sizes. Liquid "substrates" offer the necessary translational and rotational freedom for highly ordered systems.

In this approach, a thin film of a liquid is layered onto an immiscible second liquid, with CQDs dissolved in the top phase and not soluble in the bottom phase [1]. The method works well on the centimeter scale when a microliter scale volume of the top liquid is manually injected using a pipette. Automation and scaling down to the sub-mm level require a different approach to liquid handling.

In this work, the CNF Dimatix Materials printer was used to jet picoliter sized droplets of a CQD solution onto an immiscible glycol droplet (see Figure 1a). The glycol droplets were created using patterned Si substrates; the two approaches used to contain the glycol are geometric contrast (created by etching wells of the desired shape into the wafer) and wetting contrast (created by lithographic definition of wetting and nonwetting regions, as shown in Figure 1b). While the former approach provided better glycol droplet stability, the latter allows the samples to be picked up by stamping for TEM characterization, and is more suitable for prospective integration into device fabrication processes.

The approach is a modified, more complex version of that developed for the creation of ordered polymer thin films [2]. The key problem we had to solve was the choice of solvent, as any common printing additives affect the superlattice assembly. Multiple thermodynamic and kinetic constraints need to be fulfilled for the formation of high-quality films. The constrains related to the inkjet printing stem from fluid dynamics: (a) the kinetic energy has to be higher than the surface free energy so that a droplet forms, (b) the droplet acceleration, the viscous and surface forces have to be in balance so that a droplet forms and does not fall apart and (c) the same forces need to allow the droplet to break off from the jetter [3].

These constraints are expressed in terms of the dimensionless Reynolds number ($Re = \rho v d / \gamma$) and Weber-number ($We = \rho v^2 d / \mu$) as $We < 1/16\ Re^2$, $We > 1/200\ Re^2$ and $We > 4$. The numerical relations are only approximate and strongly depend on the details of the instrument. However, the general idea applies: low enough surface tension and viscosity are required for droplets to form, but the droplets have to be stabilized by high enough viscosity and surface tension.

A fourth constraint is set by the aim that the jetted droplet does not splatter the subphase droplet [4]. This is described by $We' = \rho v^2 d^3 / \gamma_s h_s^2 < 1$, where the subscript "s" indicates subphase property. Using EG, this can be converted into $We < 40$, suggesting that high viscosity and low jetting velocity are required. The constraint for spreading of the CQD solution on glycol is expressed as coefficient $S = \gamma_{02} - (\gamma_{01} + \gamma_{12})$, where 0 is air, 1 is top and 2 is bottom liquid; only a system with
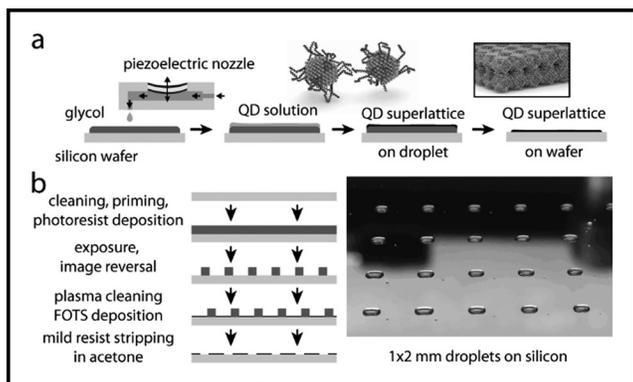
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Figure 1: a) Scheme for the interfacial assembly of CQD superlattices using inkjet printing; b) scheme for creating droplets on substrates using wetting contrast and example droplets.
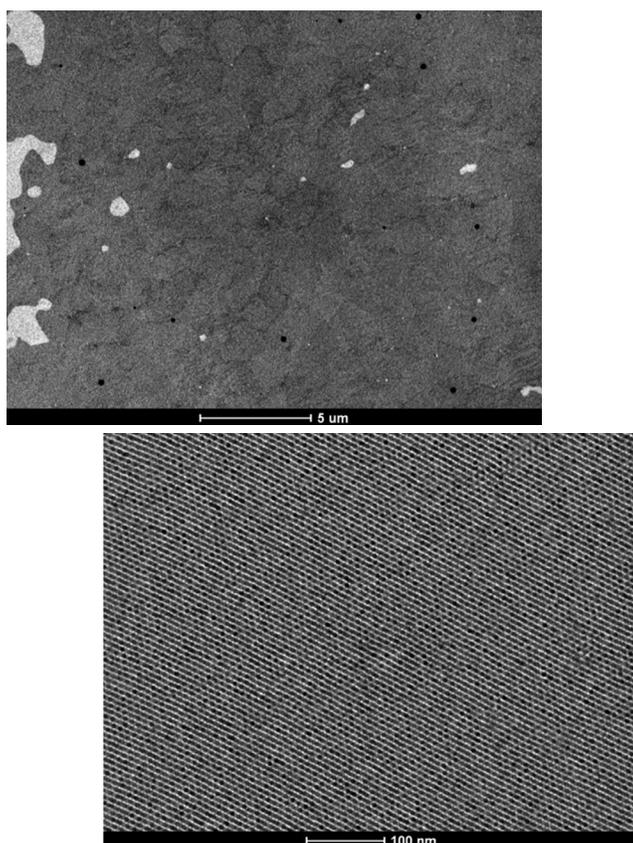
S > 0 fully spreads into a flat film. This constraint requires a solvent with low surface tension, in contrast with the high surface tension requirement of the jetting process. The final, and most important set of constraints is the immiscibility with glycol and high solubility of the CQDs. From all common solvents, alkanes with more than 10 carbon are the only suitable ones.

We performed a set of experiments with pure alkanes and their mixtures with polar solvents, and we found that dodecane is the only suitable candidate. Shorter alkanes, such as decane are not viscous enough for the jetting process (even dodecane requires a low velocity to form stable droplets), and longer alkanes do not spread well on glycol due to a high surface tension. However, we managed to optimize the jetting parameters for dodecane and the derived CQD solution without the use of additives. Example superlattices are shown in Figure 2. Good homogeneity and local order are observed in line with previous reports on large-scale samples [5].

Figure 2: Two TEM images of CQD superlattices formed on glycol droplets via inkjet printing.

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Nanoscale Periodic Pillar Feature Process Survival

CNF Project Number: 2217-13
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Primary CNF Tools Used: ASML 300C DUV, GCA 5x Autostep i-line stepper

Abstract:

The ASML 300C DUV and GCA 5x Autostep i-line stepper have been used in previous years to produce pillar and hole features with diameters ranging from 232 nm to 816 nm on fused silica and silicon wafers. Hole features are favored over pillar features because pillars are more susceptible to destruction during further wafer processing. It has been found that pillar features give optical performance up to 3.5 times higher than the hole features in spectral applications. For this reason, pillar feature fabrication with further front and backside wafer processing as well as diced die polishing was explored. For wafers that had additional metal layers patterned on the front and back side of the wafer yields of 71-79% was found with hole features and a wafer yield of 50% was found for pillar features. For wafers that had additional metal layers patterned on the front and back side of the wafer that also had an edge polished on each die after singulation had yields of 53-89% for hole features and 8% for pillar features. This reduction in wafer yield for wafers with pillars versus holes was consistent with the initial results reported last year.

Summary of Research:

In previous years a process for patterning nanophotonic pillar and hole structures was developed at CNF that used the ASML 300C DUV stepper as well as the GCA 5x Autostep i-line stepper. These features were etched into the substrate material using the patterned resist as an etch mask. The ASML 300C DUV stepper process has been used to pattern 4-inch borosilicate float glass wafers ("borofloat"), 4-inch fused silica wafers, and 4-inch silicon wafers. Pillar features like those shown in Figure 1 were fabricated with diameters ranging from 232 nm to 816 nm. Hole features were fabricated with design diameters ranging from 306 nm to 446 nm. Optimal depth of focus (DOF), exposure dose, and etch time were determined for nanophotonic patterns in fused silica by varying these parameters incrementally and examining the resultant features. Photonic crystal geometry was examined in the SEM and photonic crystal performance was assessed optically via extraction of waveguided light.

For recent applications, nanophotonic patterning was mainly focused on holes versus pillars because pillars are more likely to become damaged in a way which renders them useless for our spectral application during further processing and wafer handling. In recent years, processing steps have been added to the wafer after nanophotonic crystal pattering to include both front and back side aluminum reflector layers. These added layers can be combined with single edge polishing after die singulation as shown in Figure 2. These added steps make the pillars more exposed to handing that could damage them. It has been found that pillars designed to the same diameter of corresponding holes give spectral responsively between 50% -350% higher over a range of inputs between 400-1000 nm for designs with a diameter of 446 nm. It is because pillars give such a greater spectral responsively, that they have again been investigated for the fabrication of monolithic optical bench die design which include the light-scattering nanophotonic pattern, reflectors, and polished angular light input.

In the previous reporting period, nanophotonic pillar structures with diameters of 612 nm and 816 nm were made in fused silica wafers with the intent of seeing how they would survive further processing to produce the monolithic optical bench die design. These pillars were patterned on fused silica wafers with the ASML 300C DUV and etched into the substrate using the resist as an etch mask. The 612 nm diameter pillar wafers then had aluminum sputtered onto the front and backside which was patterned via contact lithography plus liftoff. The wafer was then coated with a protective ion beam assisted physical vapor deposited SiO$_2$ coating layer,
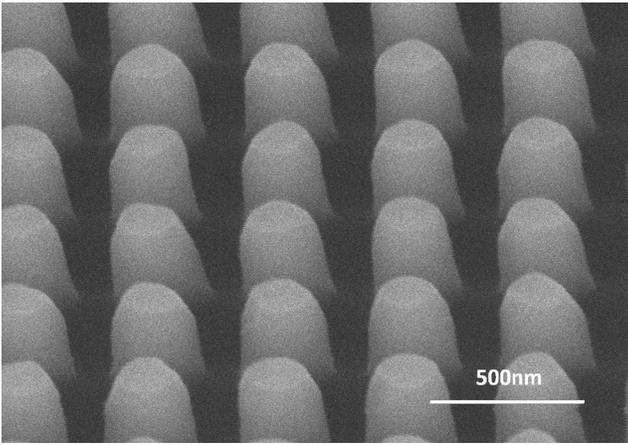
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Figure 1: SEM image of photonic crystal pattern, nominally with 270 nm pillar features, fabricated fused silica with process developed with ASML 300C DUV stepper.
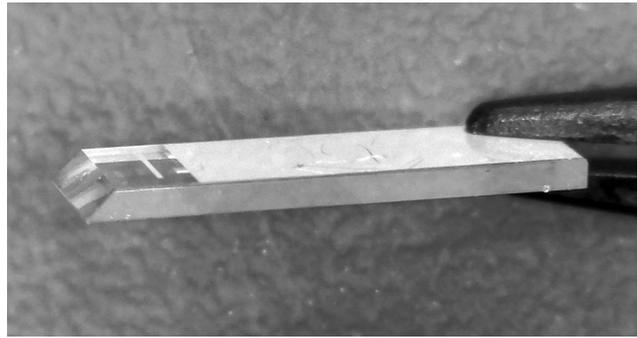

Figure 2: Diced and polished fused silica die with pattered Al reflectors on both sides in addition to the nanophotonic pattern and 45° edge polish.

Figure 3: Green light (gray) being scattered through a 306 nm diameter nanophotonic pattern illuminating pillar damage.

Wafer Percent Yield with Additional Process Steps				
Wafer #	Nanostructure Type	Hole/Pillar Diameter	Metal Lift-Off on Both Sides	Metal + Polish
1	Hole	446nm	71%	
2	Hole	408nm	79%	
3	Pillar	612nm	50%	
4	Hole	498nm		89%
5	Hole	408nm		68%
6	Hole	408nm		82%
7	Hole	408nm		53%
8	Pillar	612nm		8%

Figure 4: Wafer percent yield with additional process steps and a variety of nanophotonic pattern diameters.

diced, optionally polished and cleaned. The resulting dies were inspected by waveguiding green light into the edge of the die and inspecting the nanophotonic crystal pattern in a microscope to check for defects. Pillar damage seen in this kind of inspection is apparent in the example given in Figure 3. Nanophotonic patterns may also be rejected for other kinds of defects.

A significant drop in photonic crystal yield was found for wafers with pillar nanophotonic patterns versus holes. Yield results are listed in the Figure 4 table. Wafers that only had metal patterning on the front and back had about 25% higher yield with holes versus pillar. Wafers that had edge polishing in addition to the front and back side metal patterning had an order of magnitude higher yield for wafers with holes versus pillars.

In summary, a process to fabricate nanophotonic pillar structures with a diameter of 612 nm has been used to make dies to with further processing including front and backside aluminum patterns and singulated die polishing. Although pillar features tend to be more fragile when it comes to further wafer processing, these features tend to give higher optical throughput in spectral scattering applications in spectrometer systems.

For wafers that had additional metal layers patterned on the front and backside of the wafer yields of 71-79% was found with hole features and 50% for pillar features. For wafers that had additional metal layers patterned on the front and backside of the wafer and also had an edge polished on each die after singulation yields of 53-89% was found with hole features and 8% for pillar features.

Size Characterization of Plasma Membrane Vesicles, Virus Particles, and Synthetic Vesicles

CNF Project Number: 2575-17
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Primary Source(s) of Research Funding: National Science Foundation, National Institute of Health
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Primary CNF Tools Used: Malvern NS300 NanoSight

Abstract:

The CNF's Malvern NS300 NanoSight was used to determine the concentration and size distribution of various biologically relevant particles, including viruses and plasma membrane vesicles.

Summary of Research:

Our research investigates interactions of biologically relevant particles (viruses, microvesicles, plasma membrane vesicles) on a supported lipid bilayer and with synthetic vesicles. Most of the particles used are generated in-house and as such, it is important to characterize them (diameter, size distribution, concentration of particles) to ensure that we are using the similar quality and concentration of particles across various experiments for consistency. The concentration is especially important as too much or too little of the plasma membrane vesicles used to form the supported lipid bilayer will influence the bilayer's diffusivity and patchiness and varying concentration of viral particles may impact fluorescent dye incorporation.

Typical sizes of viruses, plasma membranes vesicles, and synthetic vesicles that we use range from 100-200 nm and typical values of concentration are on the order of 10^8 particles/mL for plasma membrane particles, 10^{10} particles/mL for viruses and 10^{12} particles/mL for synthetic vesicles.
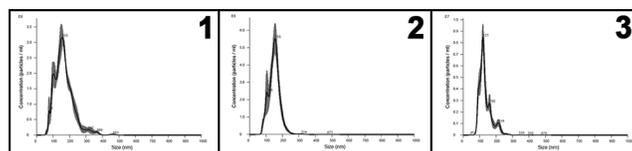

Figure 1, left: *Concentration vs. size (nm) distribution plot for virus like particles.* **Figure 2, center:** *Concentration vs. size (nm) distribution plot for pseudotyped virus particles.* **Figure 3, right:** *Concentration vs. size (nm) distribution plot for synthetic vesicles.*

Wet Etching of N-Polar AlN on NbN for Novel III-N Device Applications

CNF Project Number: 2800-19

Principal Investigator(s): Debdeep Jena, Huili Grace Xing

User(s): Jeffrey Miller

Abstract:

Typically, the highest quality thin film heterostructures achieved via epitaxial growth techniques prefer a blanket growth condition, covering the entire substrate. For device applications that demand a buried metallic layer, one must use subtractive fabrication techniques to access the buried metallic layer. In this report, we show that a KOH-based wet etch can be used to selectively etch N-polar AlN thin films with selectivity to a buried, metallic, NbN.

Summary of Research:

Over the past few decades, the III-N material system has developed into a particularly rich family of materials, playing key roles in the photonics [1], electronics [2], MEMs [3] device families — and more recently, the development of ferroelectric, magnetic, and metallic materials [4]. For III-N devices grown via epitaxial techniques, often it is preferred to grow a heterostructure or segments of a heterostructure in a blanket fashion, spanning the entire substrate. In this growth condition, one must define individual device mesas in a subtractive fashion. Recent growth efforts have shown that single crystalline wurtzite AlN can be grown on metallic, superconducting, NBN on 6H-SiC substrate by molecular beam epitaxy (MBE) [5,6]. For high frequency device applications looking to access this buried metallic NbN, but utilize a semi-insulating (SI) SiC substrate, one must etch a via through the top nitride heterostructure or through the entire SiC substrate.

Initial attempts to access the buried NbN layer via ICP-RIE etching revealed poor etch selectivity of AlN to NbN. For instance, a typical Cl- (BCl_3: 10 SCCM, Cl_2: 20 SCCM) and Ar-based (Ar72: 10 SCCM) etch in the PT 770 yielded an etch rate was $\sim$ 1 nm/s, while the epitaxial NbN layer etched at $\sim$ 2-4 nm/s under the same conditions. Over this past year, we have found one can access a buried NbN with relative ease using a two-step ICP-RIE and wet etch, overcoming the difficulty to etch 6H-SiC [7,8]. The process is shown schematically in Figure 1.
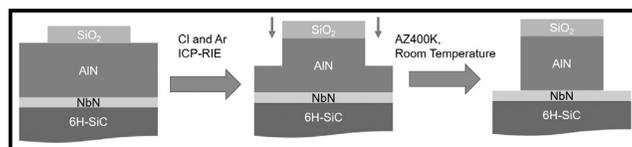

Figure 1: Schematic depiction of the two-step ICP-RIE and wet etch process. To overcome a lack of etch selectivity of AlN to NbN, etch through a small amount of remaining N-polar AlN (<200 nm) with room temperature AZ 400K.
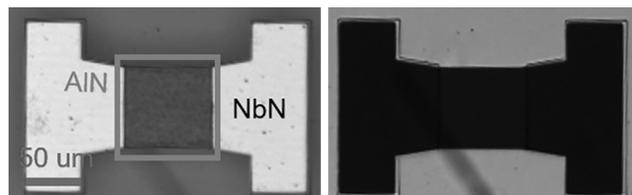

Figure 2: Optical microscope images of exposed NbN with a square AlN mesa (10,000 μm^2) post AZ 400K etch. The surrounding region is transparent 6H-SiC substrate. The thickness of the AlN mesa was 330 nm, and the height of the buried NbN was 24 nm. (a) Bright field illumination, and (b) dark field illumination. The NbN is thick enough such that it remains reflective under illumination, and the 6H-SiC substrate is optically transparent. Hence, the exposed NbN is reflective under bright-field illumination, and strongly blocks light under dark-field illumination, showing the buried NbN remains continuous under the AlN mesa.

First, the same ICP-RIE etch was applied to remove a majority of the AlN, with a PECVD SiO_2 etch mas. Then, using the same SiO_2 etch mask from the first step, the remaining (<200nm) AlN was then removed by using a dilute KOH wet etch, in the photolithographic developer AZ400K, at room temperature in under five minutes.

The exposed NbN remains conductive at room temperature, and is continuous underneath an AlN mesa.

Here, we show process results of a 330 nm thick AlN and 24 nm thick NbN heterostructure grown via MBE. Optical microscope images of the exposed NbN surface post-exposure to AZ400K are shown in Figure 2. No visible etching of the exposed NbN layer was detected, as verified by profilometry. Little lateral etching (<1μm) for AlN mesas with areas on order of 10,000 μm^2. The uniformity and speed of the etch in room temperature dilute KOH was attributed to an N-polar AlN surface (also observed by TEM in ref [6]), where KOH simultaneously serves as a catalyst in the oxidation of N-polar AlN and as a solvent for an Al_2O_3 product [8,9].

Conclusions and Future Steps:

Looking forward, we plan to see if the etch translates to N-polar GaN, and eventually more complicated III-N heterostructures. In principle, an etch selective to nitride semiconductors over metallic NbN would provide a potential pathway to dramatically scale various nitride electronics via epitaxial growth techniques. In the high frequency electronics arena, we are using the two-step etch to explore a novel bulk overtone acoustic wave resonator on 6H-SiC10 as well as a means to back-gate AlN-GaN-AlN "quantum well" high electron mobility transistors 11].

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Oxide Materials and Devices

CNF Project Number: 2802-19
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Primary Source(s) of Research Funding: Materials Science and Engineering, Cornell University
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Primary CNF Tools Used: Autostep i-line stepper, SC4500 odd-hour evaporator, PT770 etcher, P10 profilometer

Abstract:

In order to approach our research of gallium oxide lateral structure microdevices, we have worked at CNF for six months to get familiar with the gallium oxides metal oxide semiconductor field effect and fin field effect transistor processing.

Summary of Research:

In this past six months, we have been working on processing gallium oxide lateral structure microdevices, including metal oxide semiconductor field effect transistor (MOSFET), fin field effect transistor (FinFET).

MOSFET. To avoid the gallium oxide sample loss due to misoperation, an old gallium nitride (GaN) sample was used to be familiar with the standard processing. The GaN sample went through the mesa-isolation, drain and source metal deposition and metal contact annealing, shown in Figure 1a. The mesa-isolation involved photolithography and plasma etching. The metal deposition was completed by electron beam assistant physical vapor deposition. Metal contact annealing was done by the rapid thermal anneal. After the ohmic contact test, it appears that the resistance of the contact was much higher than expected. The reason could be unexpected oxidization of metal contact during the annealing shown in Figure 1b. In the rapid thermal anneal chamber, the temperature didn't reach the desired value and the ambiance didn't maintain as nitrogen along with the annealing.

With the previous experience in mind, a gallium oxide sample was processed with the same procedure. However, due to the brittle property of gallium oxides, the sample was broken during the sonication cleaning in glass beaker shown in Figure 2.

With the experience from the last two failures, the second gallium oxide sample (shown in Figure 3) was successfully processed. It was cleaned in a Teflon® beaker during sonication. We repeated the same procedure as the GaN sample. However, during the annealing process, the ambiance and temperature of the chamber were carefully controlled in a nitrogen atmosphere.

This sample showed acceptable ohmic contact of drain and source metal. The sample has deposited a layer of the dielectric layer by atomic layer deposition. The gate metal was deposited with an electron beam assistant physical vapor deposition. The contact hole was done by the wet etching.

During this processing, it's vital to ensure the photolithography alignment of building each layer. In order to achieve good alignment, the manual operation on i-line stepper was practiced several times.

FinFET. In order to study the property of FinFET with gallium oxides, one gallium oxide sample was processed with a newly designed procedure. In order to identify the electron-beam dose of the electron-beam lithography, a control sample went through the same designed procedure as the official sample, mesa-isolation, and recess etching. The mesa-isolation involved photo-lithography, metal deposition, and plasma etching. Ion milling, metal deposition, and electron-beam lithography consisted of recess etching.

Due to the lab closing for COVID-19, the official sample needs to be completed in the future.

Conclusions and Future Steps:

During the six months of work in the CNF, we mastered the basic processing techniques of gallium oxide MOSFET and FinFET, including photolithography, plasma etching, metal deposition, dielectrics deposition and wet etching. In the future, in order to complete this research of gallium oxide FinFETs, we plan to master more characterization techniques (such as atomic force morphology, scanning electron microscopy), and electron-beam lithography.
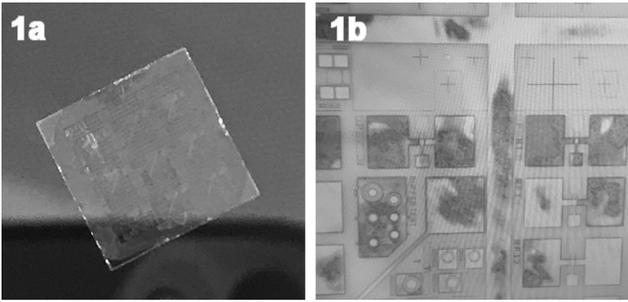
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Figure 1: After mesa-isolation, drain and source metal deposition and metal contact annealing, a) contact metal turn to a greenish color, b) oxides under the microscope.
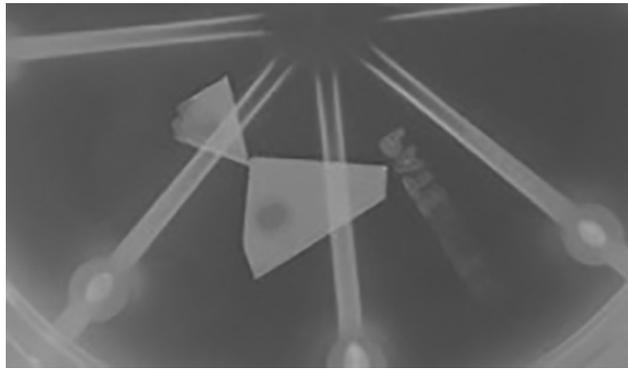

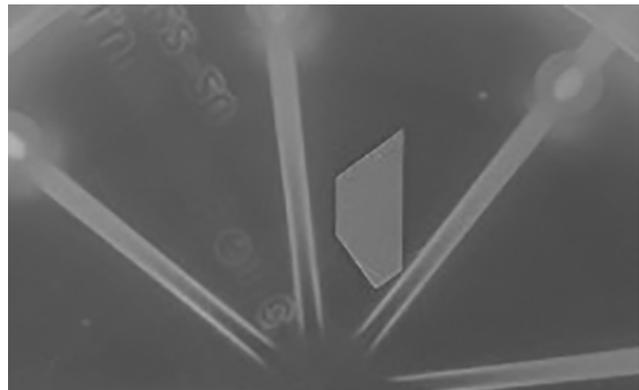Figure 2: First gallium oxides sample after sonication clean.

Figure 3: Second gallium oxide sample after sonication clean.

The Release of Thick SU-8 Films from Silicon Substrates

CNF Staff User: Aaron Windsor

Affiliation(s): Cornell NanoScale Facility, Cornell University
Primary Source(s) of Research Funding: Staff Funding/NSF
Contact: windsor@cnf.cornell.edu
Primary CNF Tools Used: ABM contact aligner, hot plates

Abstract:

For over three decades, SU-8 photoresist has been a vital tool for the fabrication of three-dimensional, high aspect ratio geometries. The resist's mechanical and chemical attributes have enabled its use throughout the many disciplines of MEMS and microfluidic research. Still, SU-8 does have a few drawbacks that have hindered its use, one being its difficulty to be removed from a substrate. There are currently many unique methods from the MEMS and electrodeposition industries for removing SU-8 off metal and silicon, but they all involve either hazardous chemicals or specialized equipment. It was discovered that thick SU-8 features could be lifted off or released from a silicon substrate after a few weeks submerged in a simple detergent bath. With proper cleaning and an overnight dehydration, a new layer of SU-8 could be reapplied on these stripped wafers. Applying different forms of mechanical force and increasing the bath temperature greatly reduced the time required to remove SU-8 and repeatedly release full SU-8 structures. This low-cost and environmentally friendly process may open new pathways for rescuing wafers, producing three-dimensional parts or devices independent of a substrate, flexible electronics and other applications.

Summary of Research:

A solution of room temperature Dawn Detergent™ and deionized water (DI) can slowly undercut the interface between thick SU-8 features and the silicon substrate wafer. Depending on the surface area, the removal of microfluidic-sized SU-8 features may require two to six weeks of soaking. The use of running water or a nitrogen/compressed air gun at an incident angle could assist with the removal of the soaked SU-8 features before they completely detach in the solution.

It was later found that increasing the temperature of the detergent solution to 95°C along with thermal cycling hastened the release process. Thermal cycling could also release SU-8 without the use of detergents.

Currently, 38 µm of SU-8 has been the thinnest SU-8 film removed using this method. It may be safe to assume that the film stress of the SU-8 combined with the surfactant undercutting action may instigate the delamination. Research is currently being done on how film stress and thickness affects this process.

In order to spin SU-8 on stripped wafers again, any traces of the detergent or residual SU-8 should be removed. Wafers were first soaked overnight in DI water and then rinsed three more times. A piranha etch was done afterwards to strip away any remaining organic residues off the substrate. The wafers were dehydrated overnight in an oven at 90°C before spinning a new layer of SU-8 on the wafer again. Some outlines of the detached SU-8 features may remain on the surface of the wafer. Repeated piranha etches may eventually remove these features, but these outlines have not affected SU-8 applications or PDMS molding.

This method was used to release large 3-D shapes from a silicon wafer. The first example was a release a complete 160 µm microfluidic device from a silicon substrate using a 200 ml DI bath with 1 ml of Triton-X at 95°C for three hours (Figure 1).

Next, an 89 µm thick, two-inch diameter spiral was fabricated with SU-8 100. Twenty-four hours after the

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post exposure bake, this wafer was placed in a room temperature DI water bath and was slowly heated 1.3°C a minute to 98°C. After one hour at the desired temperature, the wafer was removed from the bath and the SU-8 spiral was released from the wafer (Figure 2). This same wafer was again rinsed, piranha etched and dehydrated before repeating the experiment.

SU-8 was spun again, but at 1500 RPM with hopes of producing a 200 µm thick spiral (actual thickness was 178 µm). Again, the SU-8 structure was successfully removed after two total hours in the DI water bath.

In the short term, this method may be used to remove and reapply SU-8 after design changes, fabrication errors or replace essential features that are lost or broken by PDMS molding. SU-8 may be used as a quick way for fabricating prototype parts. Many ideas are currently being explored such as detachable SU-8 filters, gears and group of parts that could be released from a wafer and assembled later. Future work will focus on simulating a known UV-LIGA process of patterning SU-8 as electroplating molds and later removing the resist after depositing thick metallic films.
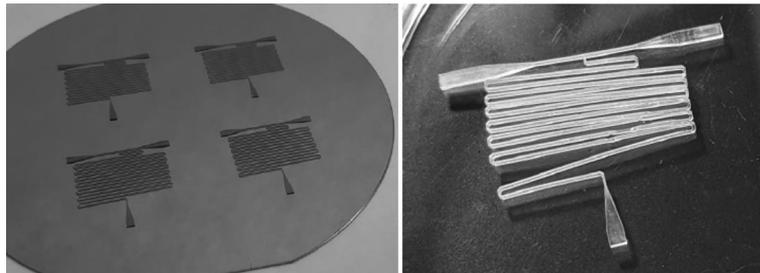

Figure 1: A complete SU-8 microfluidic device mold released from a silicon wafer. Left: Four 160 µm thick SU-8 devices patterned on a four-inch wafer. Right: Released device after submerged in heated Triton X-100 detergent solution for three hours.
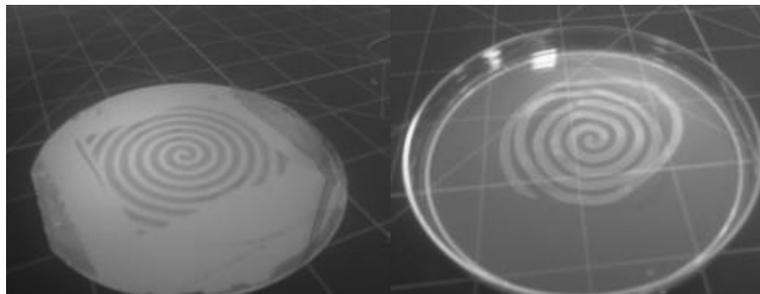

Figure 2: A complete 89 µm thick SU-8 spiral released from a silicon wafer after two hours in a DI water bath at 98°C.