Power Electronic Devices Based on Ga_2O_3

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Primary CNF Tools Used: Oxford PECVD and ALD, odd-even hour evaporation, AJA sputtering tool, PT-770 etcher

Abstract:

Gallium(III) trioxide (Ga_2O_3) is an ultra-wide bandgap semiconductor material with excellent breakdown electric field and the availability of melt-grown substrates, thus very promising for power electronic devices. Employing a vertical device topology, we have been able to successfully demonstrate Ga_2O_3 power diodes and transistors with excellent device performance, including a breakdown voltage exceeding 2 kV, as well as state-of-the-art on-state performance. Through electrostatic engineering and process optimization, we are pushing toward the limit of this material, which could surpass the performance of current power devices based on SiC and GaN.

Summary of Research:

β-Ga_2O_3 has attracted considerable interests as a promising wide-bandgap semiconductor material for power devices. Aside from the availability of melt-grown substrates, the sizable bandgap value of 4.5-4.7 eV allows for a large critical electric field exceeding 5 MV/cm as observed experimentally. Aided by the excellent field strength, high breakdown voltage exceeding 1 kV has been demonstrated in both diodes and transistors. In addition, a Baliga's figure-of-merit (BFOM) of around 0.5 GW/cm^2 has been achieved in both lateral and vertical Schottky barrier diodes (SBDs), which already exceeded the unipolar limit of Si.

Vertical power devices can provide higher current density than the lateral counterparts. With the incorporation of fin-channels, vertical enhancement-mode Ga_2O_3 transistors with good gate-control [1,2] as well as vertical Ga_2O_3 trench Schottky barrier diodes with reduced reverse leakage current [3,4] have been realized by our group.

The fabrication process for the Ga_2O_3 trench Schottky barrier diodes is as follows: First, reactive ion etch (RIE) based on BCl_3 and Ar was performed on the backside of the wafer to facilitate ohmic contact using the PT-770 etcher; After that, Ti (50 nm)/Au (125 nm) was evaporated on the backside as the cathode contact followed by a rapid thermal anneal (RTA) for 1 min under N_2 ambient; Next, Ni/Pt were deposited and patterned by a lift-off process on the top surface, serving as the Schottky contact as well as the hard mask for the subsequent etching for trench formation; Trenches with a depth of 1-2 μm were etched using RIE; Subsequently, a 100-nm Al_2O_3 dielectric layer was deposited by atomic layer deposition (ALD) using the Oxford ALD tool; Next, the dielectric was opened by dry etching to expose the Ni/Pt Schottky contact, followed by a deposition of Cr/Pt over the sidewall by sputtering using the AJA sputtering tool.

The fabrication process for the Ga_2O_3 vertical fin transistors is as follows: Si ion implantation and activation was performed in the top 50 nm of the drift layer; Pt metal masks were then patterned by electron beam lithography and deposited by electron beam evaporation on the sample surface to define position and size of the FET channels; Vertical Fin-channels were etched in the PT-770 etcher with a target width/height of 0.3/1.0 μm, respectively; Then, a 30 nm Al_2O_3 was deposited by atomic layer deposition (ALD) as the gate dielectric, followed by a 50 nm thick Cr sputtered as the gate metal; A photoresist planarization process was used

to selectively etch away the gate metal/dielectric on top of the n^+-Ga_2O_3 source; Then, a 200 nm SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) using the Oxford PECVD tool and a second planarization process was used to etch away the SiO_2 on top of the n^+ source; Finally, source ohmic contacts were formed by depositing Ti/Al/Pt, and device isolation was realized by etching away SiO_2 and Cr between active devices.

The trench Schottky barrier diodes have a specific on-resistance of 10^{-11} mW·cm^2. In comparison with the regular Schottky barrier diode, the trench diodes possess not only a lower leakage current, but also a higher breakdown voltage. In a number of 1-μm and 2-μm channel devices, the leakage current is below our measurement noise floor (1 μA/cm^2) even at a voltage of more than 2 kV. The reduction of the leakage current directly translates to the reduction of the off-state power loss.

All the vertical Ga_2O_3 MISFETs exhibit normally-off operation. The drain current reaches ~ 300-500 A/cm^2 with an associated differential on-resistance of ~ 13-18 mW·cm^2 in devices with a channel width of 300 nm. In devices with a channel width of 400 nm, the current density reaches over 1000 A/cm^2.

At off state, the device records very low drain and gate leakage currents. The 3-terminal breakdown voltage is over 1 kV. The breakdown is identified to be due to field crowding at the device periphery. With improved edge termination designs, the breakdown voltage is expected to be much higher.

In summary, we have demonstrated kV-class Ga_2O_3 power diodes and transistors. These initial device results showed a great potential of Ga_2O_3 as a promising material for power electronics applications.

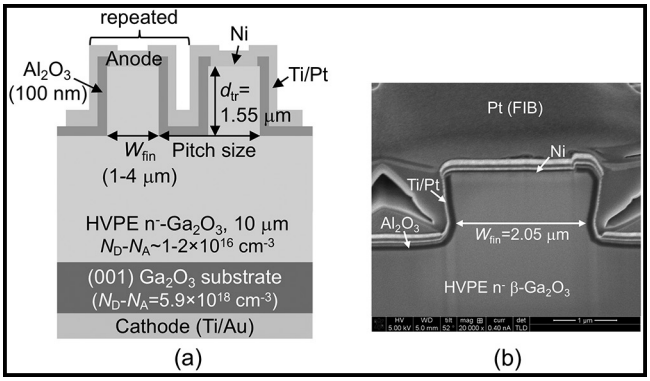

Figure 1: Schematic and SEM cross-section of the Ga_2O_3 trench Schottky barrier diodes.

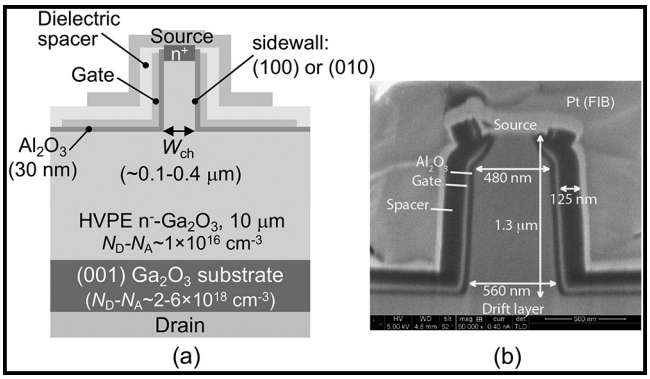

Figure 2: Schematic and SEM cross-section of the Ga_2O_3 vertical fin transistors.

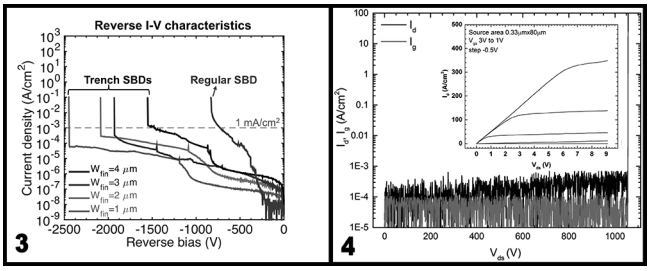

Figure 3, left: Reverse I-V characteristics of the Ga_2O_3 trench Schottky barrier diodes. Figure 4, right: Output I-V characteristics (inset) and reverse I-V characteristics of the Ga_2O_3 vertical fin transistors.

References:

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