Nanoslit Silicon Nitride Fabrication for Virus Filtration

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Primary CNF Tools Used: ASML 300C DUV stepper, SÜSS MicroTec Gamma Cluster Tool

Abstract:

Existing and widely used 0.2/0.22 µm polymer filters are not well-suited for sterilizing larger non-protein biological therapeutics during their production, as these filters entrap these molecules, thus contributing to significant yield loss. Here, we report on the fabrication of nanoslit silicon nitride (NSN) membranes with isoporous sub-0.2 µm rectangular "pores" for addressing the need for improved biological therapeutic sterile filtration. For this project, we used CNF's SÜSS MicroTec Gamma Cluster Tool and the ASML 300C DUV 4x reduction stepper, as well as various tools at Rochester Institute of Technology (RIT) Semiconductor and Microsystems Fabrication Laboratory (SMFL) to produce novel NSN sterile filters.

Summary of Research:

SiMPore produces a variety of suspended thin film membranes both porous and non-porous. For this project, the capability of the ASML 300C was explored for the fabrication of 200 nm wide slits. Capability for patterning this feature size is not available at SiMPore's home cleanroom (RIT SMFL). Prior to this project, SiMPore offered nanomembrane filters with either pore sizes ranging from 500 nm - 8 µm or sub-70 nm by way of SiMPore's NanoPorous silicon nitride (NPN) membranes, but the range in-between has been missing from SiMPore's offerings.

In this work, the SÜSS MicroTec was used to spin on 60 nm DUV 42P anti-reflective coating (ARC), then approximately 500 nm UV210 positive photoresist over 200 nm low stress silicon nitride on 150 mm diameter, 310 µm thick double side polished (DSP) wafers. The mask designed for this project had four iterations: 1:1 pitch 200 nm slits, 1:2 pitch 200 nm slits, 1:3 pitch 200 nm slits, and finally 1:2 pitch 150 nm slits. These sizes allowed exploration of strength vs. fluency as well as the ability to make slightly different sizes via over exposure, if desired. The ASML 300C was then used to expose each pattern by Focus Exposure Matrix (FEM). The resultant FEM features were then etched into the nitride, the feature sizes were measured with a Zeiss Auriga scanning electron microscope, and the optimal conditions were extrapolated. Once the conditions were selected, additional wafers were coated, exposed continuously across the entire frontside of the wafer, developed at CNF, and then taken back to RIT SMFL for further processing.

At RIT SMFL, the ARC was removed by a low power reactive ion etch (RIE) in a Trion and then the 200 nm SiN was etched via plasma etch in a LAM 490. The wafers were then stripped of the residual resist using Piranha and protected on the frontside with a silicon oxide derived from tetraethylorthosilicate (TEOS) using an AMAT Precision 5000 system. The wafers were then flipped to expose a backside pattern, etched in a similar fashion as the slit features, and then stripped. This backside pattern defined SepCon membrane chips with four (4) 0.3 mm by 3 mm porous membranes and a total chip size of 5.4 mm by 5.4 mm. Finally, the silicon wafers were bulk-etched from the backside with a crystallographic etchant and the frontside protective oxide was removed with buffered oxide etchant (BOE). See Figure 1 for process flow, and Figure 2 for scanning transmission electron microscope (STEM) images of the nanoslits.

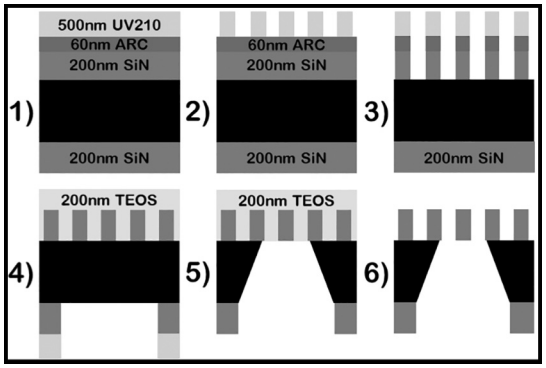

Figure 1: Process flow for NSN chips; 1) ARC plus Resist application, 2) Exposure with ASML 300C, 3) RIE of ARC and nitride to form nanoslits, 4) Frontside protection with TEOS and backside patterning, 5) Backside crystallographic etch to free-stand membranes, 6) Final porous membrane chips.

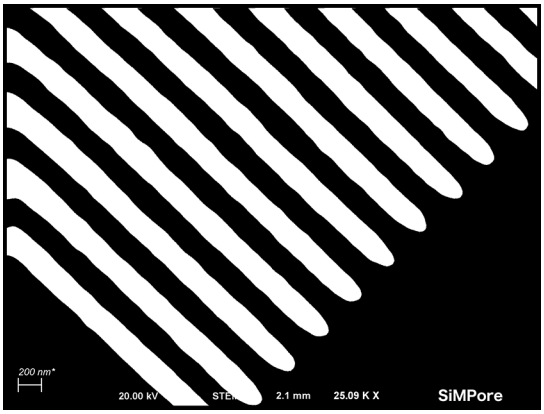

Figure 2: 25kX magnification STEM of 200 nm slits with 1:1 pitch.

One of the challenges faced in this work was the limited depth of focus (DOF) for these feature sizes. 200 nm slits are the practical limit of the 248 nm DUV light source on the ASML 300C. Due to this, we are operating at the maximum NA and Sigma, which further narrows the DOF. Another difficulty we experienced stemmed from the thinness of our wafers. The 310 µm thick wafers used for this process have considerable flex when held by a vacuum chuck (as the ASML does during exposures). The result of this is a significant loss of real estate on the final wafer, as the flexed portions of the wafer were out of focus and their features under-exposed. To combat this, our current tests use 675 µm thick wafers, and following frontside patterning, will be backside-ground and re-polished to 310 µm for subsequent bulk-etching. The resulting patterned features are significantly more uniform across the entire surface of the wafer. While there were still some aberrations; the use of ultra-flat wafers in the future may be necessary for complete and uniform exposures across a full 150 mm wafer.

In the next year, we will continue to pursue complete uniformity across these wafers, trying with tighter specified flatness, with the goal of fully useable wafers. Additionally, we will attempt using the same mask for slightly larger features to see if that will help alleviate some of the DOF issue. Our preliminary evidence suggests the 150 nm slits, when over exposed produce viable 200 nm slits at roughly 1:1 pitch.