Nanoscale Periodic Features with a 5x Autostep i-line Stepper

CNF Project Number: 2217-13
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Primary CNF Tools Used: ASML 300C DUV stepper, GCA 5x Autostep i-line stepper

Abstract:

Lithography with the ASML 300C DUV stepper has been used in previous years to produce pillar and hole features with diameters including 232 nm, 306 nm, 408 nm, and 446 nm, and with backside auto alignment on fused silica wafers. This past year, work has been furthered with the GCA 5x Autostep i-line stepper to pattern the larger of these hole features with diameters of 408 nm and 446 nm on fused silica wafers.

Summary of Research:

In previous years a process for patterning nanophotonic pillar and hole structures was developed at CNF that used the ASML 300C DUV stepper. These features were etched into the substrate material using the patterned resist as an etch mask. The ASML 300C DUV stepper process has been used to pattern 4-inch borosilicate float glass wafers ("borofloat"), 4-inch fused silica wafers, and 4-inch silicon wafers. Pillar features like those shown in Figure 1 were fabricated with diameters of 232 nm, 270 nm, 306 nm, 408 nm, 612 nm, and 816 nm. Hole features like those shown in Figure 2 were fabricated with design diameters of 306 nm, 408 nm, and 446 nm. Optimal depth of focus (DOF), exposure dose, and etch time were determined for nanophotonic patterns in fused silica by varying these parameters incrementally and examining the resultant features. Photonic crystal geometry was examined in the SEM and photonic crystal performance was assessed optically via extraction of waveguided light.

The DUV process previously developed to pattern fused silica wafers with nanophotonic pillar and hole structures was expanded to include automated backside alignment on the ASML 300C DUV stepper. Work done to enable backside alignment was achieved for up to three out of four ASML alignment marks etched into bare fused silica to a depth of 150 nm.

In previous years preliminary work was done with the GCA 5x Autostep i-line stepper to adapt the ASML 300C DUV stepper process which patterns 4-inch fused silica wafers minimum hole feature sizes of 408 nm and 446 nm. The best results of a coarse DOF and exposure dose variation study on the GCA 5x Autostep i-line stepper are shown in Figures 3 and 4. DOF and exposure dose were determined for nanophotonic patterns in fused silica by varying these parameters incrementally and examining the resultant features. The optimal etch depth used was determined in previous work making the same features using the ASML 300C DUV stepper. Photonic crystal geometry was examined in the SEM and photonic crystal performance was. Although, there is a deformity in the holes pictured in Figures 3 and 4, the optical performance of the resultant photonic crystal pattern was comparable to those seen from the DUV lithography process.

This past year a finer DOF and exposure dose variation study on the GCA 5x Autostep i-line stepper was done focusing in on those exposure parameters which gave the best performance during the coarse study. This work was focused on the hole feature sizes of 446 nm. The resultant photonic crystal patterns are being assessed via extraction of waveguided light and the best performing of these will be further examined in the SEM to determine their geometric quality.

In summary, the process previously developed to pattern fused silica wafers with nanophotonic hole structures using the ASML 300C DUV stepper was adapted to use the GCA 5x Autostep i-line stepper for hole sizes of 408 nm and 446 nm. A coarse DOF and exposure dose variation study on the GCA 5x Autostep i-line stepper resulted in photonic crystal patterns with some geometric deformation but with comparable performance to that of those made with the DUV stepper when assessed optically via extraction of waveguided light. The results of a finer DOF and exposure dose variation study on the GCA 5x Autostep i-line stepper for hole sizes of 446 nm is currently being assessed.

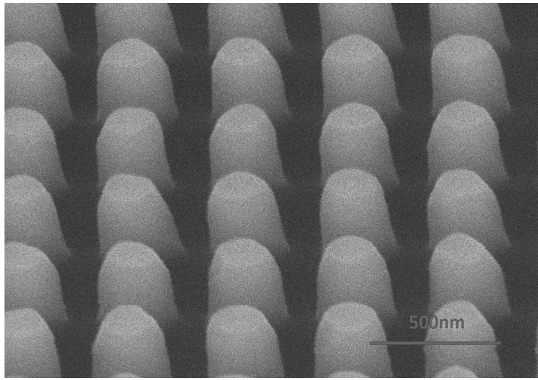

Figure 1: SEM image of photonic crystal pattern, nominally with 270 nm pillar features, fabricated fused silica with process developed with ASML 300C DUV stepper.

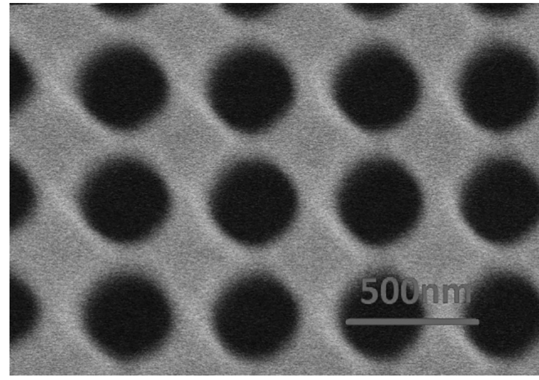

Figure 2: SEM image of photonic crystal pattern, nominally with 306 nm hole features, fabricated in fused silica with a process developed with ASML 300C DUV stepper.

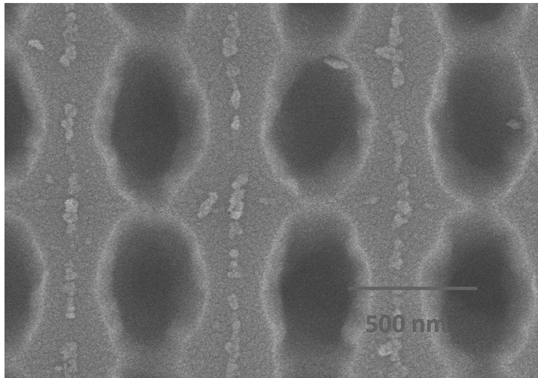

Figure 3: SEM image of photonic crystal pattern, nominally with 408 nm hole features, fabricated in fused silica with a process developed with GCA 5x stepper.

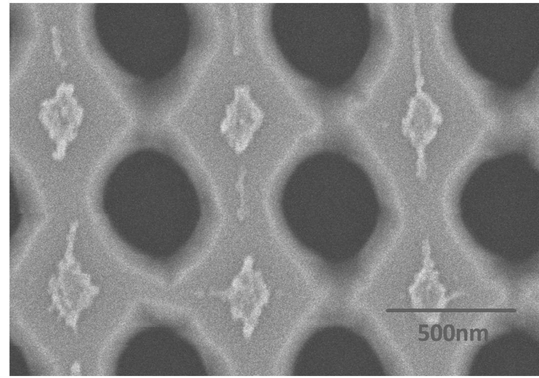

Figure 4: SEM image of photonic crystal pattern, nominally with 446 nm hole features, fabricated in fused silica with a process developed with GCA 5x stepper.

Development of GaN Vertical Trench-MOSFET with MBE Regrown Channel

CNF Project Number: 2307-14

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Users: Wenshen Li, Kazuki Nomoto, Zongyang Hu, Anni Wu, Jui-Yuan Hsu

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Primary CNF Tools Used: PT770 etcher, Autostep 200, Oxford PECVD, Oxford 81 etcher, Heidelberg mask writer DWL2000, SC4500 odd-hour evaporator, AJA sputter deposition, Oxford ALD FlexAL, DISCO dicing saw, Veeco Icon AFM

Abstract:

GaN vertical trench-MOSFETs incorporating molecular beam epitaxy (MBE) regrown channel are developed and investigated. The channel regrowth by MBE prevents repassivation of the *p*-type GaN body while promising higher channel mobility. A respectable 600 V breakdown voltage (BV) is measured in the absence of edge termination, indicating a decent critical field strength (> 1.6 MV/cm) of the regrown channel. However, the on-resistance is limited by the highly resistive lateral channel due to Mg incorporation. With an additional n^+ buried layer, excellent on-current of 130 mA/mm and on-resistivity of 6.4 mΩ·cm^2 are demonstrated, but the BV is limited by high source–drain leakage current from the channel due to drain-induced barrier lowering (DIBL) effect due to the presence of interface charge (~ 6Å ~ 10^{12} cm^{-2}) at the regrowth interface on etched sidewalls. This study provides valuable insights into the design of GaN vertical trench-MOSFET with a regrown channel, where simultaneous achievement of low on-resistivity and high BV is expected in devices with reduced interface charge density and improved channel design to eliminate DIBL.

Summary of Research:

GaN vertical power transistors have gained increasing interests in recent years due to the advantages over lateral transistors in high voltage/high current applications. Recently, a novel design based on trench metal oxide semiconductor field effect transistor (MOSFET) is realized by metal-organic chemical vapour deposition (MOCVD) regrowth of a thin GaN interlayer, which helps increase the channel mobility. Similar to the other MOCVD regrown devices, the buried Mg-doped *p*-GaN needs to be re-activated by exposing the *p*-GaN surface during high temperature anneal. This leads to high thermal budget and poses limitations on device geometry. Furthermore, any incomplete activation of buried *p*-GaN leads to reduced BV. In this report, we design a V-shaped trench MOSFET with molecular beam epitaxy (MBE) regrown unintentionally-doped (UID) GaN channel. Approximately 600 V breakdown voltage with normally-off operation is demonstrated without the need for re-activation of the buried *p*-GaN. To our knowledge, this is the highest BV achieved in GaN vertical transistors with MBE regrown channel.

The starting epitaxial structure is a high voltage *p-n* diodes structure grown by MOCVD. The schematic of the device is shown in Figure 1, which consists of a MBE regrown UID GaN channel covering the sidewall of the V-shaped trench. The conformal gate

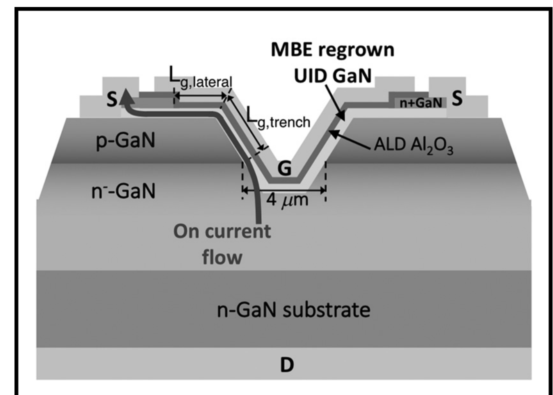

Figure 1: Schematic device structure of the GaN V-trench MOSFET.

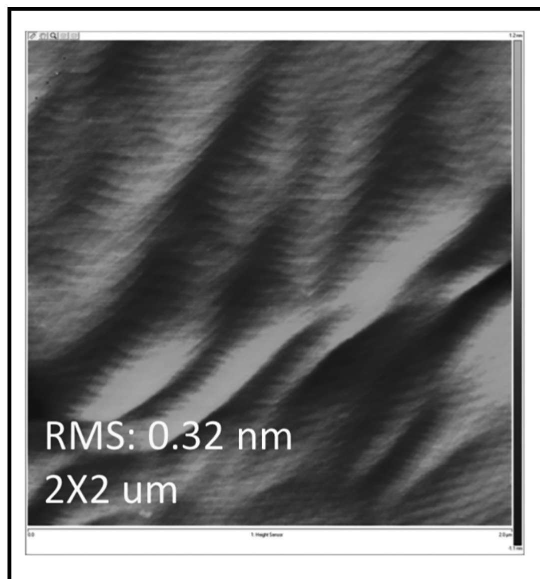

Figure 2: AFM surface morphology of the MBE regrown GaN at the trench bottom.

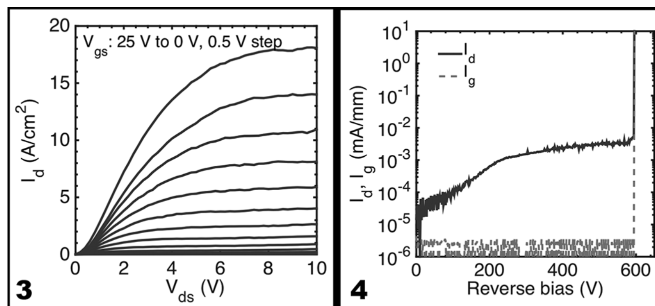

Figure 3, left: *Representative I_d-V_{ds} characteristics of a Ga_2O_3 vertical power MISFET.* ***Figure 4, right:*** *Representative three-terminal off-state (at V_{gs} = -15 V) I_d/I_g-V_{ds} characteristics and breakdown voltage of Ga_2O_3 vertical power MISFETs.*

ensures field-control of the regrown channel as well as the possible charge typically present at the regrowth interface. Smooth surface morphology of the regrown GaN at the trench bottom is observed by atomic force microscope (AFM) with clear atomic steps (Figure 2). The fabrication steps are as follows. A tapered trench is etched using our low damage Cl-based recipe on PT770 etcher with PECVD SiO_2 as mask. In order to reduce impurity concentration at the etched surface, a combination of UV-ozone cleaning and HF+HCl wet etch is performed before loading into the MBE chamber, where 50 nm UID GaN is regrown. A patterned n^+-GaN regrowth is then performed for ohmic contact purpose. Since MBE chamber has no hydrogen-containing reactants, the buried *p*-GaN remains activated. The 30 nm Al_2O_3 gate dielectric is deposited by Oxford ALD system.

The transfer curve of a single finger device shows an on-off ratio of 10^9 and normally-off operation with a threshold voltage of ~ 16 V. The output characteristics in Figure 3 show good saturation behavior and an oncurrent of ~ 18 A/cm^2 (normalized by the trench area) at V_{gs} = 25 V. R_{on} is determined from the linear region to be 0.3 Ω•cm^2. The relatively poor R_{on} and I_{on} is due to Mg diffusion in the lateral part of the channel from the *p*-GaN underneath. A thin n^+-GaN counter layer before the channel regrowth improves the channel conductivity dramatically [1]. The off-state characteristics in shown in Figure 4. Low drain leakage and a breakdown voltage of 596 V is measured with V_{gs} = −15 V, indicating good quality of the regrowth *p-n* junction interface.

In summary, record high 600 V BV is achieved among GaN vertical transistors with MBE regrown channel. No additional activation annealing of the buried *p*-GaN is needed, allowing for lower thermal budget and more flexible device geometry than MOCVD regrowth.

References:

[1] W. Li, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, and H. G. Xing, IEEE Transactions on Electron Devices 65, 2558 (2018).

[2] W. Li, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, M. Pilla, D. Jena, and H. G. Xing, in Proc. 75th Annu. Device Res. Conf. (DRC) (2017), p. 1.

Characterization of $(Al_xGa_{1-x})_2O_3$ Thin Films Grown on <010> β Ga_2O_3 by MBE

CNF Project Number: 2443-16

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Primary Source of Research Funding: NSF -Designing Materials to Revolutionize and Engineer our Future

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Primary CNF Tools Used: Veeco Icon AFM

Abstract:

Electronic devices, made of wide bandgap semiconductors, show low current leakage and high breakdown fields. Oxides of aluminum, gallium, and indium (Al, Ga and In) form a class of semiconductors with promising properties. Currently HEMT transistors, fabricated of Ga_2O_3 and $(Al_xGa_{1-x})_2O_3$ semiconductors have high breakdown voltages and low leakage currents. Hence, it is of immense interest to study and understand the growth parameters for $(Al_xGa_{1-x})_2O_3$. Here we report our preliminary growth and surface morphology results for $(Al_xGa_{1-x})_2O_3$ films grown on <010> - β phase Ga_2O_3 substrates by plasma-assisted molecular beam epitaxy (PAMBE). We correlate the growth parameters with quality and surface morphology of $(Al_xGa_{1-x})_2O_3$ films.

Summary of Research:

We grew $(Al_xGa_{1-x})_2O_3$ films with the Veeco GEN930 PAMBE system on <010> UID β Ga_2O_3 substrates at substrate temperature 500°C and O_2 flow 3 sccm. Based on AFM scans performed over a 2 μm × 2 μm sample area, the surface structure of the film is elongated along the <100> direction.

At a lower Al content, Al gets incorporated in the films smoothly and for $x < 0.2$, we observe corrugated and smooth surface having very low RMS roughness. As the Al content the layers increases above a certain limit the films become amorphous and the surface roughness increases significantly. Figures 1 and 2 indicate good surface morphologies with smooth surfaces. Figure 3 on the other hand, is for a Ga rich growth regime (high Ga BEP) which led to poor surface morphology due to Ga_2O desorption mechanism, this increased the Al incorporation in the film and made the film surface rough.

References:

[1] Kaun, S.W., F. Wu, and J.S. Speck. "β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ <010> heterostructures grown on β-Ga_2O_3 <010> substrates by plasma-assisted molecular beam epitaxy." J. of Vacuum Science and Technology A: Vacuum, Surfaces, and Films 33.4 (2015): 041508.

[2] Vogt, Patrick, and Oliver Bierwagen. "Reaction kinetics and growth window for plasma-assisted molecular beam epitaxy of Ga_2O_3: Incorporation of Ga vs. Ga_2O desorption." Applied Physics Letters 108.7 (2016): 072101.

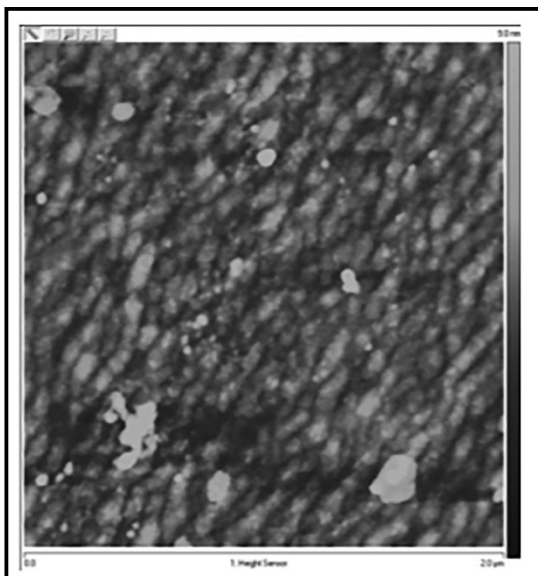

Figure 1: 2 µm × 2 µm AFM scan for Ga BEP = 3 × 10^{-9} (RMS = 1.08 nm).

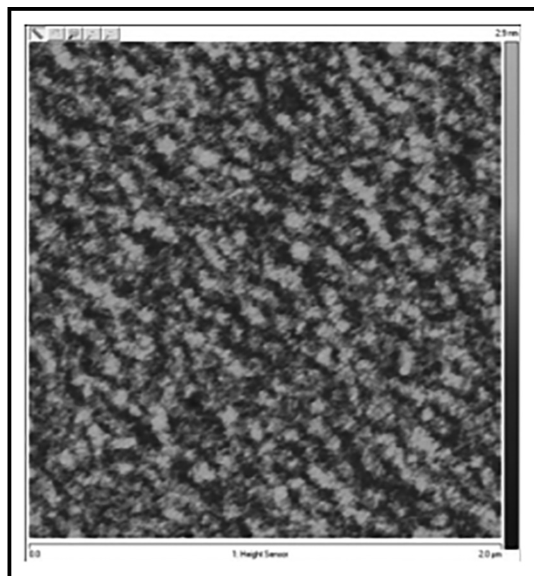

Figure 2: 2 µm × 2 µm AFM scan for Ga BEP = 5 × 10^{-9}. (RMS = 0.272 nm).

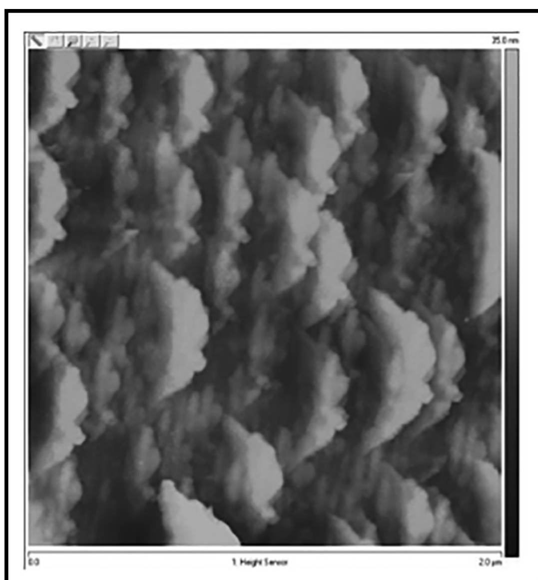

Figure 3: 2 µm × 2 µm AFM scan for Ga BEP = 30 × 10^{-9} (RMS = 4.45 nm).

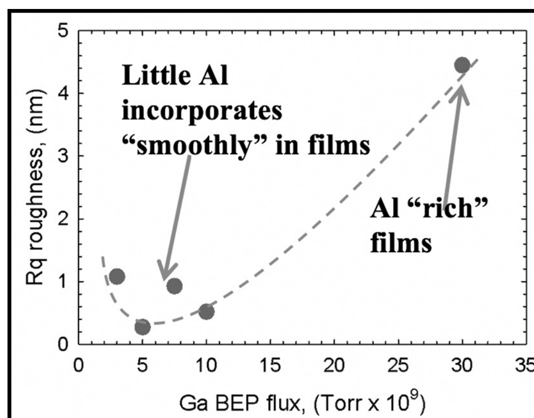

Figure 4: Graphical plot of $(Al_xGa_{1-x})_2O_3$ film roughness R_q vs Ga flux.

Device Processes and Electrical Characteristics of First 1 kV Ga_2O_3 Vertical Power Transistors

CNF Project Number: 2443-16

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Users: Zongyang Hu, Kazuki Nomoto, Wenshen Li

Affiliations: Electrical and Computer Engineering, Material Science Engineering; Cornell University

Primary Source of Research Funding: NSF, AFOSR

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Primary CNF Tools Used: Oxford PECVD, e-beam lithography tools, ICP-RIE, ALD, sputtering tools

Abstract:

High-voltage vertical Ga_2O_3 MISFETs are developed employing halide vapor phase epitaxial (HVPE) layers on bulk Ga_2O_3 <001> substrates. The low charge concentration of ~ 10^{16} cm^{-3} in the *n*-drift region allows three terminal breakdown voltages to reach up to 1057 V without field plates. The devices operate in the enhancement mode with a threshold voltage of ~ 1.2-2.2 V, a current on/off ratio of ~ 10^8, and an on-resistance of ~ 13-18 mOhm·cm^2, and an output current of > 300 A/cm^2. This is the first report of high-voltage vertical Ga_2O_3 transistors with enhancement mode operation, a significant milestone toward realizing Ga_2O_3-based power electronics.

Summary of Research:

Gallium oxide (Ga_2O_3) has emerged as a new semiconductor material for high-power applications in recent years. As the most stable form monoclinic β-Ga_2O_3 has been reported with a wide bandgap up to 4.9 eV, a high expected breakdown electric field up to 8 MV/cm and a decent intrinsic electron mobility limit of 250 cm^2/Vs, which enables high-voltage and high-power operation. The experimentally reported critical electric field up to 5.2 MV/cm already exceeds that of SiC and GaN, and electron mobility of 100-150 cm^2/Vs has been achieved in both bulk substrates as well as epitaxial layers. In addition, low-cost, large area single-crystal substrates allow high-quality epitaxial layers to be developed using various methods.

The past few years witnessed successful development of Ga_2O_3 lateral FETs including MOSFETs, MESFETs, nano-membrane FETs and FinFETs and vertical diodes such as SBDsand hetero-junction *p-n* diodes. However, high performance vertical power transistors on Ga_2O_3 have only been demonstrated by our group [1,2].

There are several reasons: (1) vertical power transistors require high quality epitaxial layers with minimized impurity incorporation and precisely controlled doping concentrations, (2) Vertical transistor structure design and fabrication processes are more complicated than those of lateral transistors and diodes.

In this report, we summarize the most recent development and results of Ga_2O_3 vertical transistors in our group.

We are able to combine high quality epitaxial Ga_2O_3 layers with a fully vertical Ga_2O_3 transistor process flow, and demonstrate the first 1-kV class vertical Ga_2O_3 MISFETs (or FinFETs). In addition to the high breakdown voltage, the transistor also shows

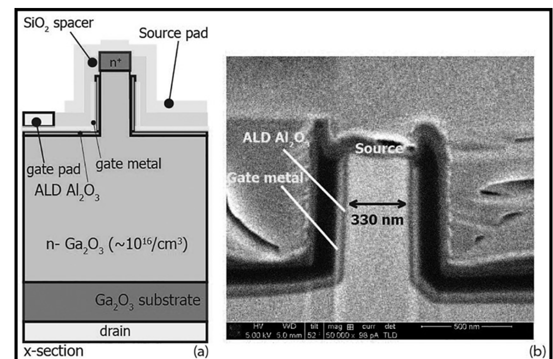

Figure 1: (a) Schematic cross-section of a Ga_2O_3 vertical power MISFET. (b) 52° SEM cross-section image of a completed Ga_2O_3 vertical Fin-MISFET showing a 330 nm wide and 795 nm long channel.

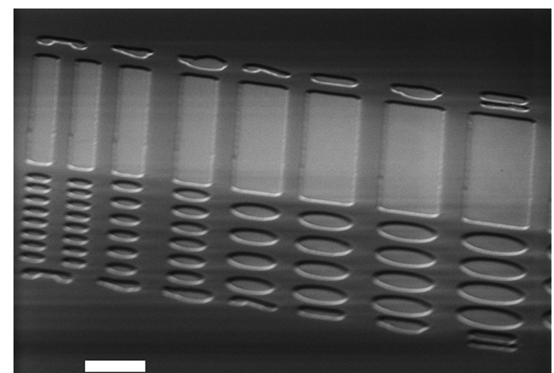

Figure 2: Representative I_d-V_{ds} characteristics of a Ga_2O_3 vertical power MISFET.

enhancement-mode operation, which is a desired feature for application as power switches.

The epitaxial layers were grown by HVPE on *n*-type bulk Ga_2O_3 <001> substrates (n = 2 × 10^{18} cm^{-3}). The 10-mm thick *n*-Ga_2O_3 epitaxial layer is doped with Si with a target doping concentration of < 2 × 10^{16} cm^{-3}.

The schematic device structure is depicted in Figure 1. A simplified process flow is described as the following:

1. Si Implantation for Top Ohmic Contacts

- SiO_2 mask deposition (Oxford PECVD)
- Si implantation with a box profile of 1E20 cm^{-3}
- Activation annealing at 1000°C in furnace

2. Vertical Channel Definition

- E-beam lithography and Pt metal mask deposition
- Low power ICP-RIE dry etching of Ga_2O_3
- Target channel width/height ratio of 0.3/1.0 μm

3. Gate Metallization

- Deposition of ALD Al_2O_3 ~ 30 nm
- Sputtering Cr ~ 50 nm to cover the sidewalls of the channel
- E-beam evaporation of Ti/Au as gate metal pads

4. Gate-Source Spacer Formation

- Photoresist planarization and thinning to expose top of Ga_2O_3 channels.
- Etch back ALD Al_2O_3 and Cr by dry etching
- PECVD SiO_2 spacer deposition ~ 200 nm
- Photoresist planarization and thinning
- SiO_2 spacer etch back

5. Source and Drain Metallization

- Sputter Ti/Al/Pt source metals
- Sputter Ti/Al/Pt back drain contacts

The net charge concentration (N_D-N_A) in the *n*-Ga_2O_3 drift layer is estimated at 1 × 10^{15} - 1.2 × 10^{16} cm^{-3} using capacitance-voltage (C-V) measurements. The low charge concentration is essential to realize E-mode operation and high breakdown voltages.

Figure 2 shows the representative I_d-V_{ds} family curves of a fabricated vertical Ga_2O_3 MOSFET with a source area of 0.33 mm × 80 mm.

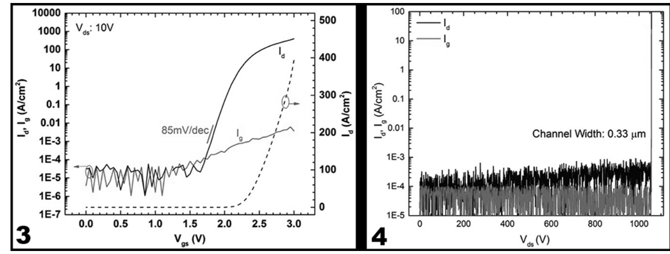

Figure 3, left: *Representative* I_d/I_g-V_{gs} *transfer characteristics in the semi-log and linear scale, along with the extracted subthreshold slope.* ***Figure 4, right:*** *Representative three-terminal off-state (at* $V_{gs} = 0$ *V)* I_d/I_g-V_{ds} *characteristics and breakdown voltage of* Ga_2O_3 *vertical power MISFETs.*

At V_{gs} of 3 V and V_{ds} of 10 V, the drain current reaches ~ 350 A/cm^2 with an associated differential on-resistance of ~ 18 mW•cm^2, normalized to the area of the $n^+Ga_2O_3$ source. The representative I_d-V_{gs} transfer characteristics of these devices are shown in Figure 3.

The V_{th} defined by linear extrapolation of the drain current at the peak transconductance is ~ 2.2 V. The sub-threshold slope is measured to be ~ 85 mV/dec near a current density of 1 mA/cm^2 and the hysteresis is less than 0.2 V. The off-state leakage currents and 3-terminal breakdown voltages in these vertical power MISFETs are measured at V_{gs} = 0 V.

The representative results are plotted in Figure 4: both the drain and gate leakage currents remain low, near the detection limit of the measurement instrument, before the hard breakdown near 1057 V. Two-dimensional device simulations reveal that the electric field peaks near the outer edges of the gate pads. In fact, examination of the devices after breakdown shows visible damage near the outer edges of the gate pads. Therefore, we expect that higher breakdown voltages be achieved by implementing field plates or ion implantation edge termination techniques.

References:

[1] Z. Hu, K. Nomoto, W. Li, L. J. Zhang, J.-H. Shin, N. Tanen, T. Nakamura, D. Jena and H. G. Xing, "Vertical fin Ga_2O_3 power field effect transistors with on/off ratio > 10^9", Device Research Conf. (DRC), pp. 1-3. DOI: 10.1109/DRC.2017.7999512, June 2017.

[2] Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena and H. G. Xing, "Enhancement-mode Ga_2O_3 vertical Transistors with breakdown voltage > 1 kV", IEEE Electron Device Lett., Vol. 39, No. 6, pp. 869-872. DOI: 10.1109/LED.2018.2830184, June, 2018.

Side-Coupled Microfluidics for Biosensor

CNF Project Number: 2465-16

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Users: Toby Mea, Zihao Wang

Affiliation: Microsystems Engineering Department, Rochester Institute of Technology

Primary Source of Research Funding: Moore Foundation

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Primary CNF Tools Used: Heidelberg mask writer DWL2000, edge bead removal system, ABM contact aligner, SÜSS SB8e substrate bonder, DISCO dicing saw

Abstract:

A side coupled microfluidic device was designed and manufactured using standard photolithography and wafer bonding technique. Devices formed from bonding two wafers using AZ 125 nXT showed satisfactory integrity, neither breaking from the dicing step or from fluid flow that was supplied using a pulled glass capillary connected to a syringe pump.

Summary of Research:

We previously designed and fabricated an iteration of a novel biosensor combining optical and microfluidic components. While the optical components displayed satisfactory performance, the previous design's microfluidic components suffered from certain critical problems that rendered it useless, including a lack of fluid perfusability and difficulty in coupling the microchannels to an external fluid supply (i.e. syringe pump). Specifically, we had previously etched microchannels into silicon dioxide and capped the microchannels using a slab of PDMS with pre-punched through holes. However, the PDMS slab was poorly bonded to the SiO_2 and the pre-punched through-holes were not properly aligned to allow fluid perfusion.

In order to overcome these limitations in the microfluidic components, we conceptualized a different approach that utilized a photoresist adhesive bonding and side-coupled microchannels (in contrast to the top-coupled microchannels from before). Before combining the optical and microfluidic components to form a complete biosensor, we created a separate standalone microfluidic device test the effectiveness of this new approach.

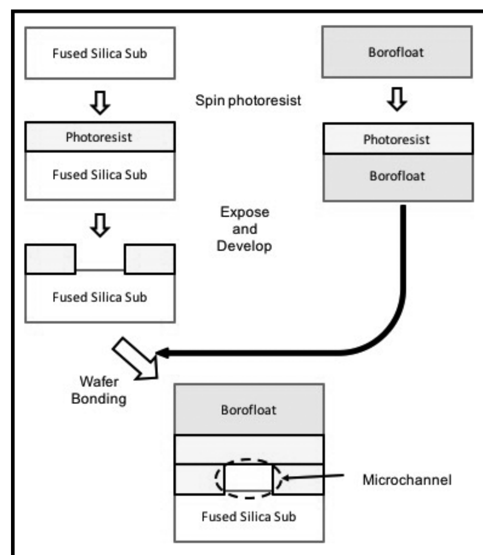

Figure 1: Process flow of fabricating side-coupled microfluidic devices.

The process flow for fabricating the standalone device is shown in Figure 1. Essentially, AZ 125 nXT is spun on a fused silica wafer to a thickness of approximately 20 μm and patterned using the ABM contact aligner, leaving behind the microchannel pattern. AZ 125 nXT was chosen because it could be spun to large thicknesses, but only one paper has extensively documented its use for micromachining [1]. We then spun and exposed AZ 125 nXT on a second wafer made of borosilicate glass. AZ 125 nXT is broadband sensitive, which

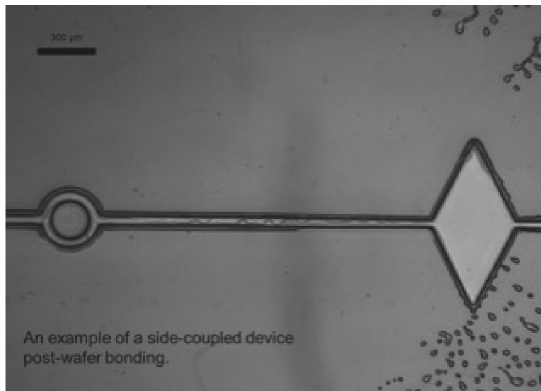

Figure 2: Micrograph showing side-coupled microfluidic device after wafer bonding.

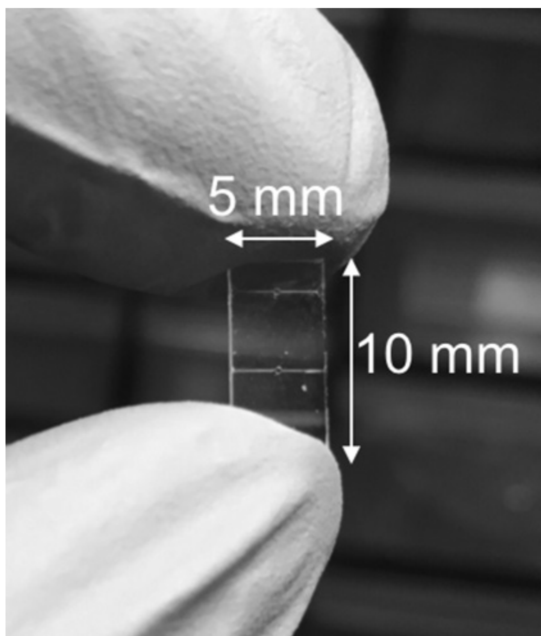

Figure 3: Snapshots of the completed side-coupled microfluidic device.

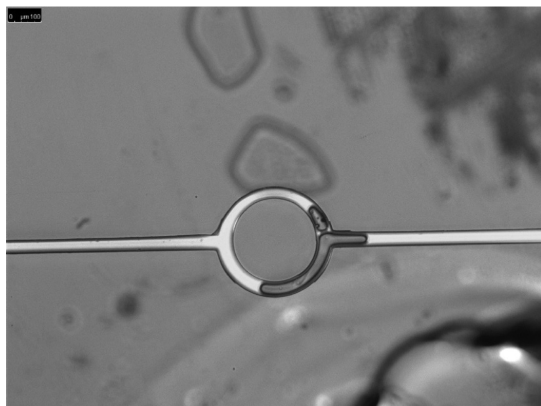

Figure 4; Snapshots of fluid perfusion through microchannels.

effectively cut the necessary exposure from the ABM contact aligner by a factor of 3. The two wafers were then bonded together using the SÜSS substrate bonder. Specifically, the two wafers were heated to 100°C and pressed against each other with a force of 1000 N to form the final device wafer. Upon bonding, the patterned photoresist showed minimal deformation, leaving the microchannels clearly defined (shown in Figure 2). Finally, using the DISCO dicing saw, the device wafer was diced into individual devices (shown in Figure 3). The wafers did not separate during the dicing step, which indicated good bonding between the wafers.

The resulting devices were then subjected to fluidic tests to investigate the perfusability of the device and the feasibility of side-coupled microfluidics. To couple the microchannels to an external syringe pump, 1 mm glass capillaries were pulled using a glass pulling machine to achieve a tip with a diameter that could fit into the microchannel inlet/outlet. In addition to being able to fit the tips into the inlet/outlet, the tip could also perfuse fluid supplied from a syringe pump (shown in Figure 4).

Pumping fluid from the syringe pump revealed that the microchannels were capable of perfusing fluid up to flows of 250 μL/hr. Therefore, we have successfully designed and fabricated a side-coupled microfluidic device that can effectively perfuse fluid.

Although side-coupled microfluidic devices have already been reported in the literature (mostly for mass spectroscopy purposes [2-3]), these experiments nonetheless demonstrated that side-coupling may be a viable strategy for realizing the microfluidic components on our proposed biosensor.

References:

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[2] S. Koster, and E. Verpoorte, "A decade of microfluidic analysis coupled with electrospray mass spectroscopy mass spectrometer: an overview", Lab Chip, vol. 7, pp.1394-1412, 2007.

[3] Z. L. Fang, and Q. Fang, "Development of low-cost microfluidic capillary-electrophoresis system coupled with flow-injection and sequential-injection sample introduction", Fresenius J. Anal. Chem., vol. 370, pp.978, 2001.

Size Characterization of Plasma Membrane Vesicles, Virus Particles, and Microvesicles

CNF Project Number: 2575-17
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Affiliation: Chemical and Biomolecular Engineering, Cornell University

Primary Source of Research Funding: National Science Foundation

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Primary CNF Tools Used: Nanosight

Abstract:

Nanosight was used to determine the concentration and size distribution of various biologically relevant particles, including viruses and plasma membrane vesicles.

Summary of Research:

Our research investigates interactions of biologically relevant particles (viruses, microvesicles, plasma membrane vesicles) on a supported lipid bilayer. Most of the particles used are generated in-house and as such, it is important to characterize them (diameter, size distribution, concentration of particles) to ensure that we are using the similar quality and concentration of particles across various experiments for consistency. The concentration is especially important as too much or too little of the plasma membrane vesicles used to form the supported lipid bilayer will influence the bilayer's diffusivity and patchiness. Typical sizes of viruses and plasma membrane vesicles that we use range from 100-200 nm and typical values of concentration are on the order of 10^8 particles/mL (for plasma membrane particles) and 10^{10} particles/mL for viruses.

After characterizing the particles, they are most often used to study the particle interaction on a supported lipid bilayer under total internal reflection fluorescence microscopy (TIRFM). TIRFM only excites fluorophores within 100 nm so we can distinguish between particles that are interacting with the bilayer versus particles that are in the bulk solution.

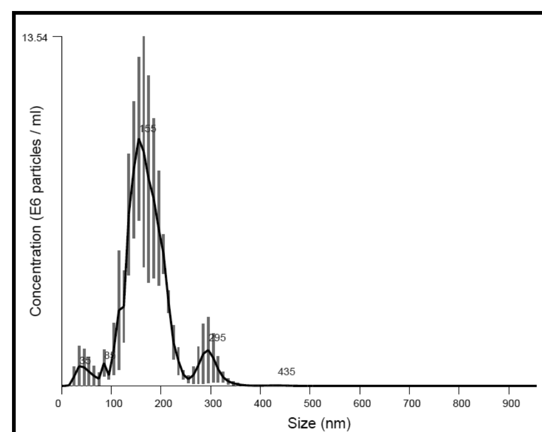

Figure 1: Concentration vs. size (nm) distribution plot for pseudotyped virus particles.

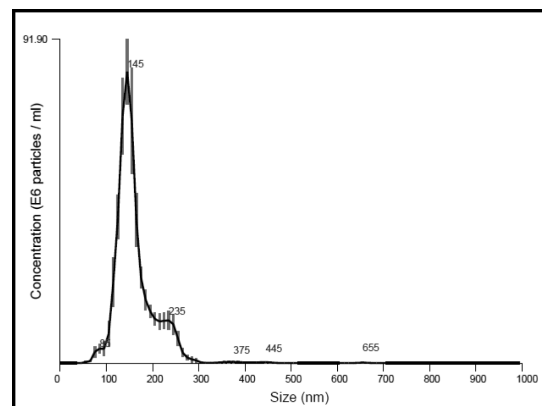

Figure 2: Concentration vs. size (nm) distribution plot for plasma membrane vesicles.

Hard Mask Fabrication from Block Copolymer Templates and Atomic Layer Deposition

CNF Fellows Project

Principal Investigators: Vince Genova[3], Alan Bleier[3]

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Primary Source of Research Funding: National Science Foundation (Grant ECCS-1542081)

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Primary CNF Tools Used: Oxford FlexAL ALD, Zeiss SEM, Oxford Cobra etcher, YES Asher

Abstract:

Block copolymer (BCP) lithography enables facile self-assembly of nanostructures at size scales inaccessible by optical lithography. We demonstrate tone-reversal and hard mask creation from BCP templates by utilizing the conformal nature of atomic layer deposition (ALD) of alumina. The alumina enables creation of hard masks that possess high etch selectivity. We demonstrate the utility of this process by fabricating high-aspect-ratio silicon nanowires with 30 nm lateral dimensions and 180 nm vertical dimensions.

Summary of Research:

Block copolymer (BCP) resists create nanoscale features through phase segregation of dissimilar polymer blocks. A variety of morphologies including pores, pillars, and lines have been demonstrated through choosing appropriate copolymer blends [1]. A challenge for the community is design of resists that possess high selectivity during etching and thermal processes. One approach is to incorporate silicon-containing compounds into the resist, such as polystyrene-polydimethylsiloxane (PS-PDMS) blends. Our approach, however, is to convert the resist pattern into a hard mask using conformal atomic layer deposition (ALD). This approach enables tone-reversal of substrate patterns and offers a broad palate of materials for the mask creation. The versatility of this approach enables device engineers to choose a hard mask with the desired etch properties.

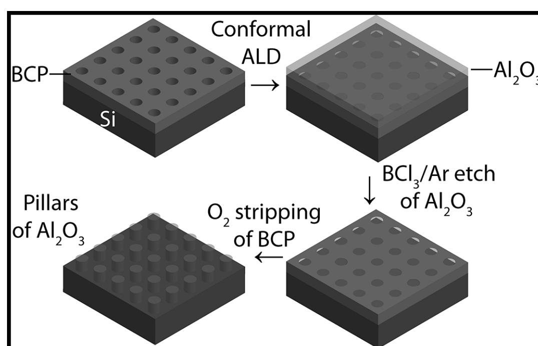

Figure 1: Process flow for hard mask creation from block copolymer templates.

The process flow for creating of hard masks from BCP templates is outlined in Figure 1. A BCP blend of polystyrene and poly-methylmethacrylate (PS-PMMA) is used as a template. The PS-PMMA ratio chosen produces a morphology of pores in the resist. Low-temperature ALD of alumina conformally coats the features and self-planarizes by over-filling the pores. Directional etching of the over-filled alumina produces a pattern of alumina-filled pores in the BCP template. Finally, the BCP resist is stripped in a downstream oxygen plasma, leaving behind alumina pillars.

The process was characterized through visual inspection in the scanning electron microscope (SEM). Figure 2 (top) shows the formation of the pores in the BCP resist. Typical pore sizes range between 25-30 nm. The total resist thickness is comparable to the pore size. The bottom micrograph in Figure 2 shows the wafer decorated with the remaining alumina pillars.

Optimization of the alumina etching time is essential to avoid eroding the mask. The results presented are 300 cycles of ALD alumina (nominal thickness 30 nm) and an alumina etching time of 1.5 minutes at 25 nm per minute. A slight over-etch guarantees that all of the over-filled alumina has been removed, while still remaining safely within the process window for the alumina pillar.

To demonstrate the utility and etch resistance of the alumina masks, we fabricate arrays of silicon nanowires

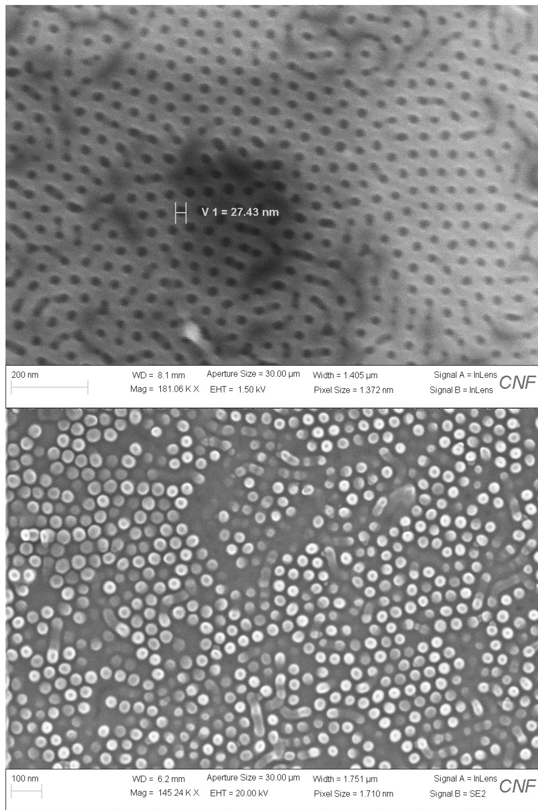

Figure 2: Scanning electron micrographs (SEMs) of the BCP tone reversal process.

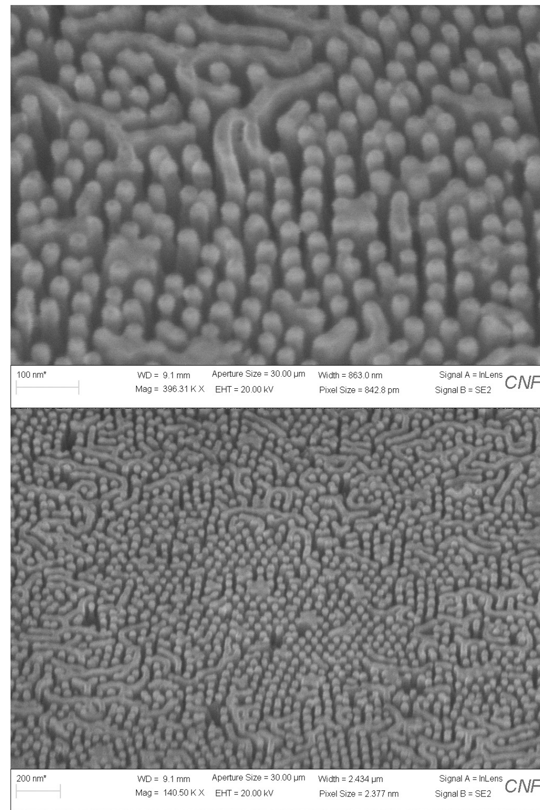

Figure 3: SEMs of high-aspect-ratio silicon nanowires fabricated from alumina masks.

by etching in an HBr/Ar plasma. Figure 3 shows successful fabrication of silicon nanowires with 30 nm diameters and heights approaching 180 nm. Pattern transfer is uniform across large areas, and is only limited by the defect density in the BCP resist. Many lithographic approaches toward vertical nanowire fabrication involve costly electron-beam lithography steps, while this approach is facile, versatile, and enables high aspect ratios. Optimization of the nanowire etch could further increase achievable aspect ratios in this system.

The ease of fabrication of silicon nanowires with high aspect ratios inspires device concepts and applications. The fabricated structures have dimensions and packing densities smaller than visible optical wavelengths. The reflectance therefore approaches zero, as there are no smooth surfaces for reflection of light. Therefore, by doping the top layer of silicon, vertical *p-n* junction solar cells can be fabricated that do not suffer from reflection losses.

References:

[1] Jeong, Seong-Jun, Ju Young Kim, Bong Hoon Kim, Hyoung-Seok Moon, and Sang Ouk Kim. "Directed Self-Assembly of Block Copolymers for next Generation Nanolithography." Materials Today 16, no. 12 (December 1, 2013): 468-76. https://doi.org/10.1016/j.mattod.2013.11.002.

Photocurable Nanoimprint Lithography (P-NIL): An Enabling Technology for MEMS and Nanophotonics

CNF Fellows Project

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Website: https://confluence.cornell.edu/display/CNFUserWiki/UV+Nanoimprint+Process+using+mr-XNIL26+resist

Primary CNF Tools Used: Nanoimprint NX-2500, MVD 100, Oxford 82 etcher, Unaxis 770 deep Si etcher, Oxford Cobra ICP etcher, SEM

Abstract:

We evaluate a new photocurable imprint resist (mr-XNIL26) from Microresist Technology and develop a working photocurable nanoimprint process on various substrates using the Nanonex NX-2500 imprint tool.

Summary of Research:

Nanoimprint lithography (NIL) is an emerging technology that has the advantage of high throughput with sub-10 nm resolution. The resolution is largely governed by the feature dimensions of the master or template, which can be defined by advanced photolithography or electron beam lithography. NIL has been a strategic method on the ITRS roadmap for the 45 nm node and below. In addition to electronics, NIL can be a benefit to many applications including nanophotonics, biotechnology, displays, and microelectromechanical systems.

The Nanonex NX-2500 has both thermal imprint (T-NIL) and photocurable imprint (P-NIL) capabilities. The photocurable imprint module uses 200W narrow band UV lamp. A quartz template was fabricated by sputter depositing a blanket layer of chrome in which a bright and dark field line space pattern was defined with the ASML DUV (248 nm) stepper producing a minimum feature size of 250 nm. The lithographically defined pattern was then transferred into the chrome using Cl_2/O_2/Ar mixed chemistry in the Trion inductively coupled plasma (ICP) tool. This etch produces smooth and perfectly anisotropic sidewall profiles, which are essential for optimum imprint replication. The chrome is used as a hard mask to etch the quartz substrate to a depth slightly less than the mr-XNIL26 resist thickness in the Oxford 80 reactive ion etching (RIE) tool using CF_4. The chrome is then removed by immersing the substrate in liquid chrome etchant. The template is coated with FOTS in the molecular vapor deposition (MVD) system to prevent the adherence of the resist in the imprint process. The Microresist Technology P-NIL resist system evaluated was mr-XNIL26, which is a new fluorine-modified UV nanoimprint resist with advanced release properties. We applied the mr-XNIL26-300 nm to a silicon wafer along with Omnicoat as an adhesion promoter, although the adhesion promoter is not necessary. The imprint is performed at room temperature and at a pressure of only 10 psi which is low compared to a thermal imprint process. The UV cure time is 30 seconds. The single layer P-NIL process is illustrated in Figure 1 adopted from Microresist Technology.

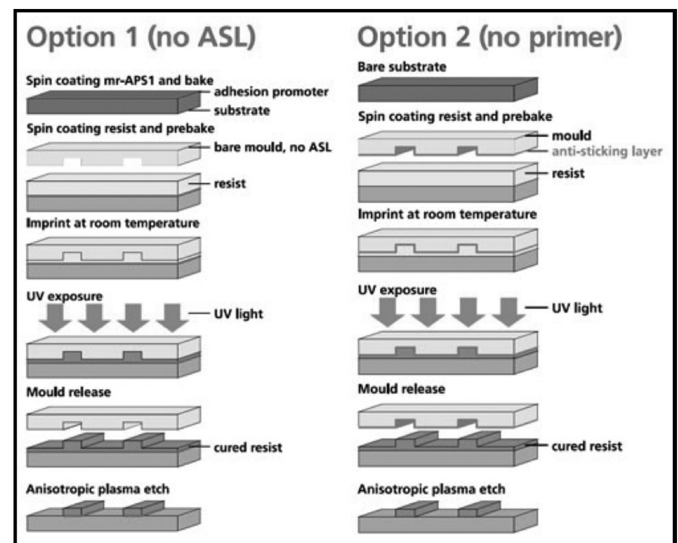

Figure 1: mr-XNIL26 P-NIL process overview from Microresist Technology.

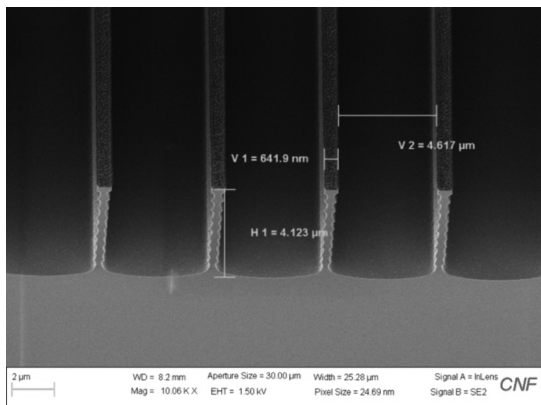

Figure 2: Bosch etch in Plasma-Therm SLR-770 of 600 nm features to an aspect ratio of 9:1.

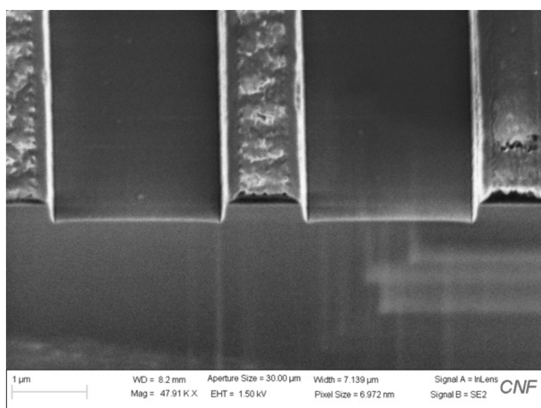

Figure 3: Oxford Cobra HBr silicon etch with a 4:1 selectivity of silicon to mr-XNIL26.

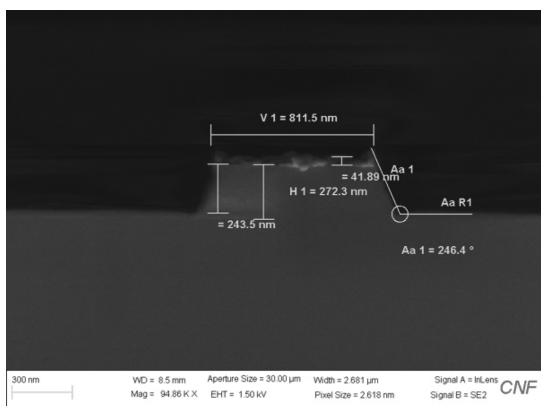

Figure 4: Silicon nitride etch using CH_2F_2/He in Oxford 100 ICP.

We used option 1 where Omnicoat® was used as an adhesion layer in place of mr-APS1. Residual layer etching is performed in the Oxford Plasmalab 80 using oxygen at low pressure (15 mTorr) and low power (50W) to retain critical dimensions and minimize the loss of resist. The post-imprint residual thickness layer is largely dependent on pattern density and feature size. The imprinted silicon wafers were etched with the Bosch deep silicon etch and the mixed SF_6/C_4F_8 etch in the Plasma-Therm SLR ICP. An additional wafer was etched with HBr in the Oxford Cobra ICP. The Bosch etch is commonly used in the fabrication of MEMS devices, while the mixed etch and the HBr etch are used for nanophotonics based devices. The P-NIL process using mr-XNIL26 resist was also applied to a silicon nitride layer.

Pattern transfer into Si_3N_4 was accomplished in the Oxford Plasmalab 100 ICP using CH_2F_2/He chemistry. This dielectric etch is used in the fabrication of oxide and nitride based nanophotonics devices here at CNF.

Figure 2 illustrates the results of the Bosch deep silicon etch for feature sizes of 600 nm etched to an aspect ratio of 9:1. The selectivity of silicon to the mr-XNIL26 resist is about 40:1, comparable to standard DUV and i-line photoresists. For the silicon etching with SF_6/C_4F_8 chemistry in the Plasma-Therm SLR-770, the selectivity of silicon to the mr-XNIL26 is 3:1, slightly less than standard DUV and i-line resists.

In Figure 3, we show the results of silicon etching in the Oxford Cobra ICP using HBr. Both the SF_6/C_4F_8 and the HBr etches produce highly anisotropic profiles with smooth sidewalls. Results of pattern transfer into silicon nitride using CH_2F_2/He in the Oxford 100 ICP are shown in Figure 4. The CH_2F_2/He chemistry is highly polymerizing and therefore highly selective with respect to imprint and conventional photoresists. The detailed process flow is posted on CNF user Wiki for reference.

In conclusion, we have evaluated a new photocurable imprint resist (mr-XNIL26) from Microresist Technology on our Nanonex NX-2500 imprint tool. This single layer resist system has been studied and the removal of residual resist has been optimized with proper plasma etch chemistry and parameters. We have then demonstrated effective pattern transfer into both silicon and silicon nitride using advanced ICP based reactive ion etching. We are currently working on combing e-beam lithography pattern and DUV pattern on one single template for imprint demonstration. We believe this process shows great potential in the fabrication of MEMS and photonics-based devices.

PS-PMMA Block Copolymer Lithography for Sub-25 nm Periodic Features

CNF Fellows Project

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Website: https://confluence.cornell.edu/display/CNFUserWiki/Block+Copolymer+Resist

Primary CNF Tools Used: ABM contact aligner, Oxford 80s, PT72, ULTRA/SUPRA scanning electron microscope (SEM), Hummer Au/Pd sputtering system, PMMA spinners, vacuum ovens, wet chemistry

Abstract:

Nanolithography is a fundamental requirement for the future of electronics patterning. Current trends indicate the end of Moore's Law for traditional lithography processes. Directed self-assembly (DSA) of block copolymers (BCPs) can generate ordered, periodic arrays of various structures down to single nanometer (nm) size scale. The heterogeneous nature of these structures acts intrinsically as their own mask, enabling nm scale resolution with a flood exposure and no traditional photo mask. BCP lithography offers low-cost processing of nm scale periodic structures typically only available by e-beam lithography and can act as a complementary technology to conventional photolithography. In this work, we develop a PS-*b*-PMMA BCP lithography process on SiO_2/silicon using CNF labs and tools, achieving ~ 20 nm pattern resolution.

Summary of Research:

BCP lithography relies on the microphase separation of the two comprising polymers to achieve a nanoscale pattern. Due to the reliance on self-assembly, the resulting photolithographic features are intrinsically periodic. As such, this process is useful for applications in areas where long range repeating structures are needed, such as nano-porous substrates, nanoparticle synthesis, or high-density information storage media.

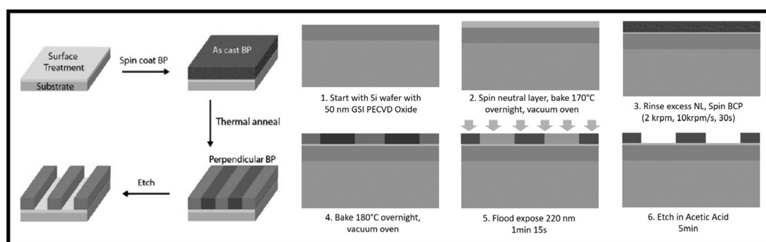

Figure 1: Left: Typical BCP lithography fabrication flow (adapted from [1]). Right: Fabrication flow for PS-b-PMMA BCP.

For the development of this method, we used a poly(styrene-*block*-methyl methacrylate) (PS-*b*-PMMA) *block* copolymer due to its popularity in literature, which stems from its excellent etch selectivity, low surface energy mismatch, and theoretical 12 nm feature size.

The typical fabrication flow for a BCP lithographic process is shown in Figure 1 (left) (adapted from [1]). First, a surface treatment is applied to create a neutral layer/brush. This prevents a surface parallel BCP domain orientation from occurring by making the substrate surface interfacial energy equal for both polymer phases. Next, the BCP is spin-coated and then thermally annealed allowing for phase separation and formation of the pattern. Finally, one phase is selectively removed, and subsequent substrate processing can occur from this point.

We used P9085-SMMAranOHT as our neutral layer and P8205-SMMA as our BCP (both obtained from Polymer Source). Our process flow follows that shown in Figure 1 (right), where the etch is accomplished using a 220 nm flood exposure followed by an acetic acid dip. Various polymer concentrations, film thickness, and anneal conditions were tested for their effect on pattern formation (morphology, uniformity, periodicity, etc.) and optimized. For detailed information and considerations, see the CNF User Wiki article [2]. Figure 2 shows SEM micrographs of the BCP at various points in fabrication for an approximately 25 nm thick film.

To quantify the effect of our parameter sweeps, it was necessary to develop an image processing technique that could quickly evaluate samples. We used ImageJ to develop two separate macros for; 1) measuring

feature sizes and 2) evaluating inter-feature spacing. In our case, the BCP morphology is a hexagonal array of pores, so these methods were tuned to generate information on pore diameter and interpore spacing. The former was accomplished using built in ImageJ functions and the Particle Analysis tool. The latter is comprised of built in ImageJ functions along with an additional macro for K-Nearest Neighbor analysis that was expanded on from an existing implementation, as well as a custom Matlab script [3]. Again, the CNF Wiki Article has more detailed information and output examples of this image analysis.

Through this system of evaluation, we were able to achieve BCP films of 30 nm thickness with long range order. Pore sizes of ~ 23.12 nm with 1.78 nm standard deviation and interpore spacing of ~ 54.26 nm with 7.33 nm standard deviation and a circularity of ~ 0.92 were obtained. Figure 3 shows example SEM images of a typical sample. Using these films, pattern transfer through 50 to 100 nm of oxide has been achieved, as well as a subsequent Si etch (Figure 4).

In the future, we are working on various path forwards for BCP lithography implementation at the CNF. One path is further process tuning to reduce defects in the film and improve uniformity and periodicity. Beyond this, we are also looking into additional processing steps required to alter the BCP film morphology. We are working on a graphoepitaxy process that will result in parallelly aligned domains, rather than pores. Finally, we are also investigating other BCP systems for smaller features sizes (< 10 nm), such as PS-*b*-PDMS.

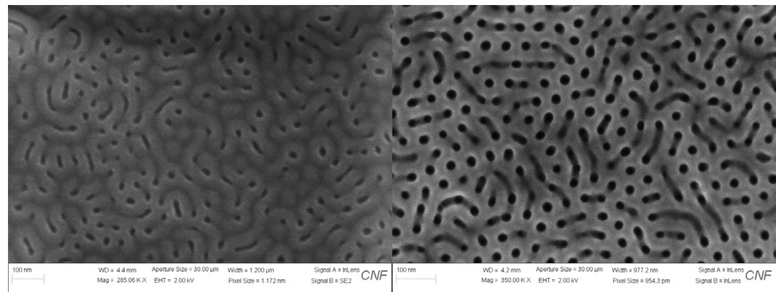

Figure 2: SEM micrographs of BCP film. Left: after annealing. Right: after etching. The increase in contrast comes from the removal of the PMMA phase in the pore regions after the etch.

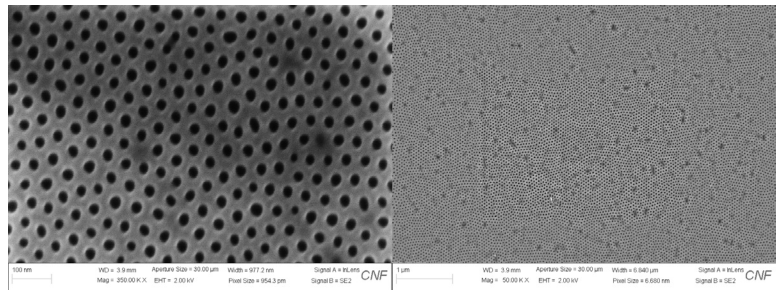

Figure 3: SEM micrographs of optimized BCP film. Left: 350kx magnification showing pore diameter and interpore spacing uniformity. Right: 50kx magnification showing long range order.

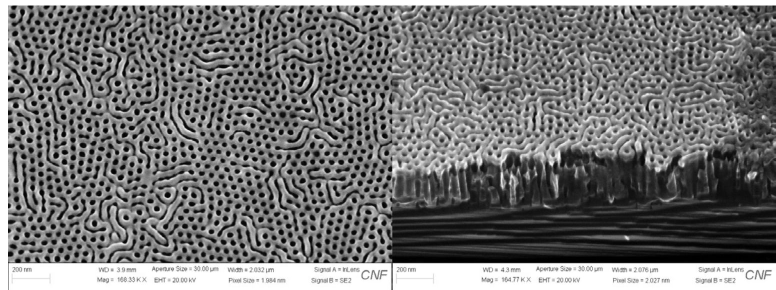

Figure 4: SEM micrograph of BCP on 50 nm of SiO_2 on Si after CH_2F_2/He and HBr/Ar etch. Left: Top down. Right: Cleaved, 45 degrees.

References:

[1] C.M. Bates, et al., Block Copolymer Lithography, Macromolecules, 2014, 47 (1), pp 1-12.

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[3] Burri, Olivier, 2D K Nearest Neighbors Python script, GitHub repository, https://gist.github.com/lacan/2643f2ce7e33d1bb07adafde9ff94101 (2017).